Kontron User's Guide

DIMM-PC®/520-I/IE/IU

Document Revision 1.26

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1 User Information

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2 Introduction

2.1 Important Information

This user guide provides information about all three versions of the DIMM-PC/520. Below is a list of the corresponding article numbers for each version. Each version may be equipped with different options of onboard memory and onboard IDE compatible Flash hard disk.

- 08012-xxxx-xx-0 DIMM-PC/520-I
- 08012-xxxx-xx-1 DIMM-PC/520-IE (with Ethernet)
- 08012-xxxx-xx-2 DIMM-PC/520-IU (with USB)

Note: That the DIMM-PC/520 may be equipped with either the Ethernet feature or the USB feature. At this point in time Kontron does not produce a version of the DIMM-PC/520 that has both of these features.

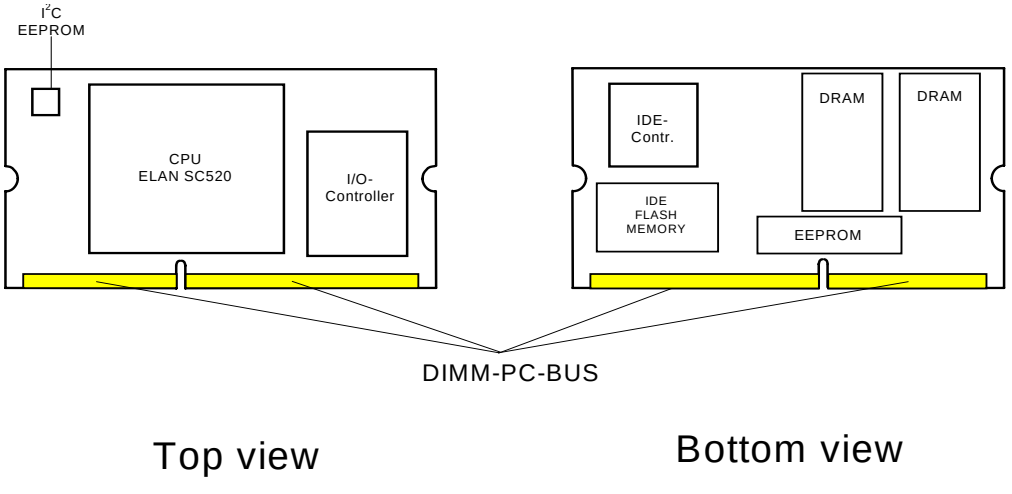
When reading this user guide the user must be aware of which version of the DIMM-PC/520 they have. The information within this user guide covers all three versions of the DIMM-PC/520.When certain information, within this user guide, only applies to a particular version of DIMM-PC/520 then it will be stated.

For example: **Universal Serial Bus (USB) (Available only on DIMM-PC/520-IU)**

2.2 DIMM-PC/520-I/IE/IU

The DIMM-PC/520-I/IE/IU integrates the complete functionality of an ElanSC520 board, offering a CPU, system BIOS, 16/32 DRAM, keyboard controller, real-time clock, and a 16/32MB IDE compatible onboard Flash hard disk. The Elan solution includes a highly integrated embedded CPU chip made by AMD.

DIMM-PC modules are designed for embedded applications with industrial BIOS extensions such as setup-date in EEPROM as a host-mode function, allowing operation with an external PC as terminal.



The pinout of the DIMM-PC bus connector corresponds in large part to the pinout of a standard ISA bus. Only the latchable address bus LA [17..23] and DMA signals 1,3,4, and 6 are not connected to the DIMM-

PC bus. The DIMM-PC bus of the DIMM-PC/520-I/IE/IU offers peripheral functions such as COM1, COM2, LPT1, floppy interface, and IDE hard-disk interface.

2.3 DIMM-PC Architecture

The application-specific portion of a standard embedded application typically requires low pin count components such as relays, power supplies and A/D-converters. An embedded PC requires components of much higher pin-count and higher density circuit boards. The DIMM-PC concept separates the high-density circuit board of the embedded PC from the low density, often two-layer, application-specific baseboard.

To simplify the connection of the peripheral components, such as A/D converters, a programmable chip-select-signal has been defined on the DIMM-PC bus. This chip-select-signal can be adjusted in the BIOS setup of the PC for corresponding I/O addresses. With a single external TTL component, up to eight I/O components can be triggered. In the regular ISA bus, the user has to connect 20 pins to a GAL to select an external component. The programmable chip select decodes unnecessary ISA bus address signals. This makes triggering the external bus-buffer components possible.

To address the drawback of a higher price for a PC solution, the DIMM-PC performs without discrete peripheral connectors, significantly reducing the cost. In other PC solutions, such as PC/104, connectors and their assembly are a significant part of the manufacturing costs. In "low end" 386SX-solutions, these costs can be as much as 25%. Because the DIMM-PC performs without connectors, these costs are significantly decreased and the PC can be integrated on a smaller board surface. The reduction in the number of steps necessary in manufacturing and assembling the component group is another cost-decreasing factor.

The two-sided reflow process, as well as exclusion of the wave-solder process, serves to increase the yield in manufacturing and improve quality. The required SO-DIMM connector is a very inexpensive, standard component and is available from numerous manufacturers.

In designing the DIMM PC, attention was directed toward its use in embedded applications. Moreover, its design was developed in co-operation with large-scale customers. Because most peripheral interfaces used in such applications are device-internal (in external interfaces, mainly special customized interfaces are used), the RS232 interface driver components have been excluded from the DIMM-PC, leading the interfaces as pure TTL signals to the outside. This further decreases additional costs, while enabling the user to have more flexibility when selecting the interface driver (RS485, RS422, RS232, TTY etc.). The power consumption of the PC architecture is drastically reduced with integrated components. This makes the system optimally adaptable with power-saving modes.

The PC in the DIMM-PC architecture also has minimized or eliminated some of the most critical disadvantages of the microcontroller:

- The DIMM-PC today needs less board surface than most micro-controller applications.
- The embedded PC cost has been drastically decreased by the DIMM-PC architecture.
- The DIMM-PC architecture has eliminated the complicated cabling of an embedded PC.

The user receives important advantages by using a DIMM-PC. Because of the 100% PC-compatibility, the user can begin the software development immediately on a standard PC. This is a factor that may influence the success of a product in today's market, where "time to market" is of high importance. As target hardware becomes available, it can be implemented with no obstacles to operation because it will be unnecessary to change the software. With the SO-DIMM-connector, an exchange for a more powerful type CPU is possible, increasing the scalability of the ultimate device. In the case of product information and new designs, the CPU may simply be superseded by a new DIMM-PC, saving redesign time. Through continuous development of the DIMM modules, the cost for the life span of a product can be reduced, profiting users. The integrated IDE controller allows the user to work with normal PC tools with no need for hardware-specific drivers.

3 Specifications

3.1 Functional Specifications

Processor

- Elan SC520 with AM5x86TM CPU core, 16K write-back cache, floating point unit, 100MHz or 133 MHz

Onboard DRAM memory

- Up to 32MB, clocked at 66MHz

Onboard IDE compatible Flash hard disk with 16MB/32MB (IDE master)

Two serial port interfaces: COM1 and COM2

- TTL signals, 16550 compatible

One parallel port interface (LPT1)

- EPP support

Floppy interface

Universal Serial Bus (USB) (Available only on DIMM-PC/520-IU)

- One USB 1.1 ports (OHCI)

Onboard Ethernet: Intel 82551ER PCI single chip(Available only on DIMM-PC/520-IE)

- 10BASE-T LAN

IDE hard-disk interface (external hard disk as slave)

Real-time clock

Keyboard controller

EEPROM for CMOS setup

I²C Bus (slave devices only)

5V-only power supply

ISA electrical characteristics (such as timing and DC characteristics)

- Support for IRQ9, 10, 11, 12 and 15 for peripheral functions
- Support for DMA channel 0 for peripheral functions; DMA channel 7 is not available

- Master, Refresh and 0WS mode are not supported

Programmable /CS output

3.2 Mechanical Specifications

The interconnection of a DIMM-PC board is achieved by plugging the board to the DIMM connector in a peripheral application. Following are the dimensions of the DIMM-PC board and a DIMM connector. Please refer to the Kontron DIMM-PC specification for additional information.

3.2.1 PCB Dimensions

- 67.6 mm x 40 mm (2.66" x 1.57")

3.2.2 Height

- 6 mm max

3.3 Electrical Specifications

3.3.1 Supply Voltage

- 5V DC +/- 5%

3.3.2 Supply Voltage Ripple

- 100 mV peak to peak 0 – 20 MHz

3.3.3 Suspend Supply Current (Typical)

- Suspend mode not supported

3.3.4 Supply Current (Nominal value)

- 620mA (at 133MHz CPU clock)

3.3.5 Supply Current from Battery (Max.)

- < 6µA @ 3V battery, 0..70°C, no system power
- < 3µA with system power on

3.4 Environmental Specifications

3.4.1 Temperature

- Operating: 0 to +65 C (*) (with appropriate airflow)
- Non-operating: -40 to +80 °C (non-condensing)

Note: *The maximum operating temperature is the maximum measurable temperature on any spot on the module's surface. You must maintain the temperature according to the above specification.*

3.4.2 Humidity

- Operating: 10% to 90% (non-condensing)
- Non-operating: 5% to 95% (non-condensing)

4 CPU, Chipset, and Super I/O

4.1 CPU

The DIMM-PC/520-I/IE/IU uses an Elan SC520 with an AM5x86TM CPU core. It features 16K write-back cache, floating-point unit, and runs at speeds of 100MHz or 133 MHz.

4.2 Chipset

The Elan™SC520 is a full-featured microcontroller developed for the general embedded market. The Elan™SC520 combines a 32-bit, low-voltage AM5$_x$86 CPU with a set of integrated peripherals suitable for both real-time and PC/AT-compatible embedded applications

4.3 Super I/O

The Winbond W83977A super I/O offers support for floppy disk controller, two serial ports, one parallel port, and PS/2 keyboard controller.

5 System Memory

The DIMM-PC/520-I/IE/IU contains 8, 16, 32, and an optional (upon request) 64MB of DRAM, which are integrated onboard.

6 ISA Bus

The DIMM-PC/520-I/IE/IU supports the PC/104 16-bit ISA bus. The pinout of the DIMM-PC bus connector corresponds to the pinout of the ISA bus connector. The Latchable Address (LA) bus [17-23] and DMA signals 1, 3, 4, and 6 are not connected to the DIMM-PC bus.

6.1 Signals

6.1.1 SD<0:15>: System Data Bus

Bi-directional I/O pins.

This refers to signals that provide data bus bits 0 to 15 for peripheral devices. All 8-bit devices use SD<0:7> for data transfers. The 16-bit devices use SD<0:15>. To support 8-bit devices, the data on SD<8:15> will be gated to SD<0:7> during 8-bit transfers to these devices. The 16-bit CPU cycles convert into two, 8-bit cycles for 8-bit peripherals.

6.1.2 SA<19:0>: System Address

Output from CPU modules and input to all other modules.

This refers to address bits 0:15 that address I/O devices. Address bits 0:19 address system memory. The 20 address lines, in addition to LA<17:23>, allow access of up to 16MB of memory. SA<0:19> are gated on the PC/104-bus when BALE is high and latched to the falling edge of BALE.

6.1.3 /SBHE: System Bus High Enable

This refers to output on CPU modules and input to other modules. The signal /SBHE indicates a transfer of data on the upper byte of the data bus (SD<8:15>). The 16-bit I/O devices use /SBHE to condition data bus buffers tied to SD<8:15>.

6.1.4 BALE: Bus Address Latch Enable

This refers to output from CPU modules and input on other modules. The signal BALE is an active high pulse, which generates at the beginning of a bus cycle that is initiated by a CPU module. It indicates when the SA<0:19>, LA<17:23>, AEN, and /SBHE signals are valid.

6.1.5 AEN: Address Enable

This refers to output from CPU modules and input to other modules. The signal AEN is an active high output that indicates a DMA transfer cycle. Only resources with an active /DACK signal should respond to the command lines when AEN is high.

6.2 Control Signal Group

6.2.1 /SMEMR: System Memory Read

This refers to output from CPU modules and input to other modules. The signal /SMEMR instructs memory devices to drive data onto the data bus. The signal /SMEMR is active on memory-read cycles to addresses below 1MB.

6.2.2 /SMEMW: System Memory Write

This refers to output from CPU modules and input on other modules. The signal /SMEMW instructs memory devices to store the data present on the data bus. The signal /SMEMW is active on all memory-write cycles to addresses below 1MB.

6.2.3 /IOR: I/O Read

This refers to output from CPU modules and input on other modules. The signal /IOR instructs an I/O device to drive its data onto the data bus. The CPU or DMA controller may drive the data. The signal /IOR is inactive (high) during refresh cycles.

6.2.4 /IOW: I/O Write

This refers to output from CPU modules and input on other modules. The signal /IOW instructs an I/O device to store present data on the data bus. The CPU or DMA controller may drive the data. The signal /IOW is inactive (high) during refresh cycles.

6.2.5 /IOCHCK: I/O Channel Check

This refers to output from CPU modules and input on other modules. The signal /IOCHCK is an active, low-input signal that indicates an error has taken place on the module bus. If /IOCHCK is enabled on the CPU module, an /IOCHCK assertion by a peripheral device generates a non-maskable interrupt (NMI) to the processor.

6.2.6 IOCHRDY: I/O Channel Ready

This refers to output from CPU modules and input on other modules. The IOCHRDY is pulled low to extend the read or write cycles of any bus access when required. The CPU, DMA and refresh controllers can initiate the cycle. The default number of wait states for cycles initiated by the CPU is 4 for 8-bit peripherals and 1 wait state for 16-bit peripherals. One wait state is inserted as default for all Direct Memory Access (DMA) cycles. Peripherals that cannot present read data or strobe in write data in this amount of time use IOCHRDY to extend the cycles.

This signal should not be held low for more than 2.5 us for normal operation. Any extension to more than 2.5 us does not guarantee proper DRAM memory contents because memory refresh is stopped while IOCHRDY is low.

6.2.7 /MEMCS16: 16 Bit Memory Chip Select

This refers to input to CPU modules and open collector output on other modules. The /MEMCS16 signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done when the CPU module requests a 16-bit memory cycle and the /MEMCS16 line is high. If the /MEMCS16 line is high, 16-bit CPU cycles are automatically converted into two, 8-bit cycles on the bus. If /MEMCS16 is low, an access to peripherals is done via a 16-bit wide cycle.

6.2.8 /IOCS16: 16 Bit I/O Chip Select

This refers to input to CPU modules and open collector output to other modules. The /IOCS16 signal determines when a 16-bit to 8-bit conversion is needed for I/O-bus cycles. A conversion is done when the CPU module requests a 16-bit I/O cycle and the /IOCS16 line is high. If /I/OCS16 is high, 16-bit CPU cycles are converted into two, 8-bit cycles on the bus. If /I/OCS16 is low, access to peripherals is done via 16-bit wide cycle.

6.2.9 /REFRESH: Memory REFRESH

This refers to output to CPU modules and input to other modules. /REFRESH pulls low whenever a refresh cycle initiates. A refresh cycle activates every 15.6 us to prevent loss of DRAM data.

6.2.10 /0WS: 0 Wait States

This refers to input to CPU modules and output to other modules. The 0 wait-state signal tells the CPU to complete the current bus cycle without inserting default wait states. By default, the CPU inserts four wait states for 8-bit transfers and one wait state for 16-bit transfers.

6.3 Special Function Signal Group

6.3.1 /MASTER

This signal is internally connected and is not to be used by external devices.

6.3.2 SYSCLK: System Clock

This refers to output from a CPU module and input to other modules. SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with 40-60 percent duty cycle. Different CPU modules can supply slower and higher frequencies. This signal is supplied at all times except when the CPU module is in sleep mode.

6.3.3 OSC: Oscillator Frequency

This refers to output from CPU modules and input to other modules. CPU modules supply OSC. They have a nominal frequency of 14.3 MHz and a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.

6.3.4 RESETDRV: Bus RESET

This refers to output from CPU modules and input to other modules. This active high output is system-reset generated from CPU modules to reset external devices.

6.3.5 DRQDMA Request

This refers to CPU modules and outputs from other modules. External devices use the asynchronous DMA request inputs to indicate when they need service from the CPU modules' DAM controllers. DRQ<0:3> are used for transfers between 8-bit, I/O adapters and system memory. DRQ<5:7> are used for transfers between 16-bit, I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on CPU modules.

6.3.6 /DACK: DMA Acknowledge

This refers to outputs from CPU modules and inputs to other modules. DMA acknowledges 0-3 and 5-7 acknowledges DMA requests. They are low active.

6.3.7 T/C: Terminal Count

This refers to output from CPU modules and input to other modules. The active high output TC indicates that one of the DMA channels has transferred all data.

6.3.8 IRQ: Interrupt Requests

This refers to input to CPU modules and output to other modules. These are asynchronous interrupt request lines. IRQ0, 1, 2, 8 and 13 are not available as external interrupts because they are used internally on CPU modules. All IRQ signals are active high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt-service routine).

7 Serial Communication Interface

The DIMM-PC/520-I/IE/IU has two 16550 compatible serial ports, with TTL-level signals. You can configure the ports as COM1 and COM2.

7.1 Configuration

You can set the COM1 and COM2 serial ports to the base I/O-address 3F8h, 2F8h, 3E8h, 2E8h, or disabled. The serial ports are compatible with the serial-port implementation used on the IBM Serial Adapter. You can set the interrupts to INT3 – INT4. You can modify all base I/O-addresses and interrupts in the BIOS setup menu.

7.2 Signals

7.2.1 DTR#: Data Terminal Ready

This signal refers to the active-low, data-terminal ready outputs for the serial port. A handshake-output signal notifies the modem that the Universal Asynchronous Receiver/Transmitter (UART) is ready to establish a data-communication link.

7.2.2 RI#: Ring Indicator

This signal refers to the active-low input for the serial port. A handshake signal notifies the UART that the modem has detected a telephone ring signal.

7.2.3 TXD: Transmit Data

This signal refers to the transmitter serial-data output from the serial port.

7.2.4 RXD: Receive Data

This signal refers to the receiver serial-data input.

7.2.5 CTS#: Clear To Send

This signal refers to the active-low input for the serial port. A handshake signal notifies the UART that the modem is ready to receive data.

7.2.6 RTS#: Request To Send

This signal refers to the active-low output for the serial port. A handshake signal notifies the modem that the UART is ready to transmit data.

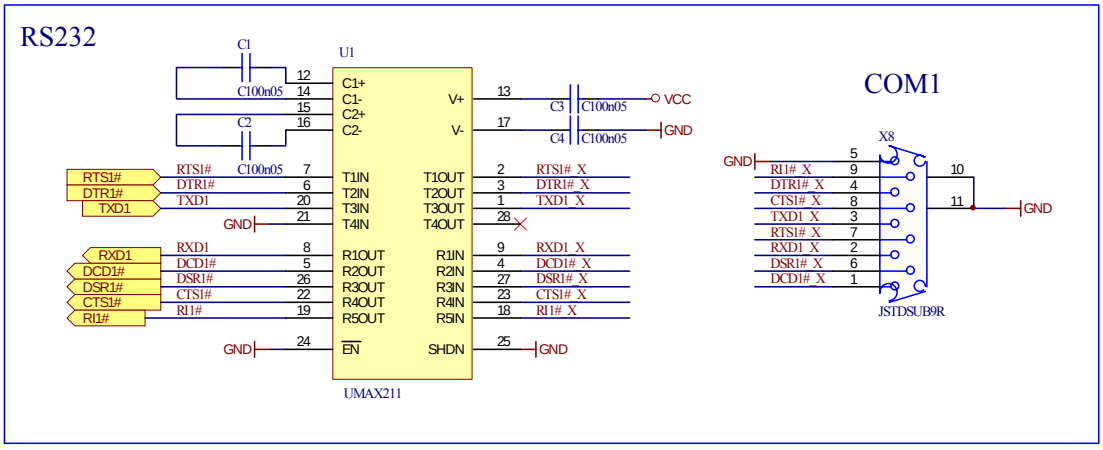
7.2.7 DCD#: Data Carrier Detect

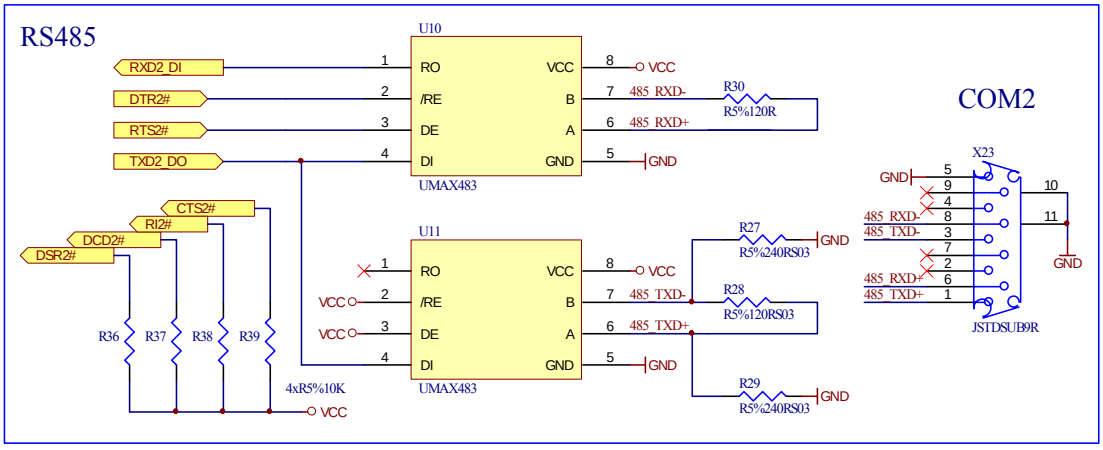
This signal refers to the active-low input for the serial port. A handshake signal notifies the UART that the modem has detected a carrier signal.

7.2.8 DSR#: Data Set Ready

This signal refers to the active-low input for the serial port. A handshake signal notifies the UART that the modem is ready to establish a communication link.

7.3 Design Example





8 Parallel Port Interface

The DIMM-PC/520-I/IE/IU supports one parallel port (LPT1). This port maintains full compatibility with the PC/AT printer port and adds PS/2 bi-directional capability.

8.1 Configuration

The BIOS setup automatically configures the port. The parallel port's base I/O port address settings are 3BCh, 378h, 278h, or Disabled. The parallel-port mode settings are Normal and Extended. You can change the settings in the BIOS setup.

8.2 Signals

8.2.1 STB#: Strobe Signal

The active low pulse strobes the printer data into the printer.

8.2.2 AFD#: Auto feed Output

The active low output causes the printer to automatically feed one line after each line is printed.

8.2.3 PD [0-7]: Printer Data Bus

The bi-directional parallel data bus transfers information between the CPU and peripherals.

8.2.4 ERR#: Error

The active low signal indicates an error situation at the printer.

8.2.5 INIT#: Initiate Output

The active low signal initiates the printer when low.

8.2.6 SLIN#: Printer Select Input

The active low signal selects the printer.

8.2.7 ACK#: Acknowledge

The active low output from the printer indicates it has received the data and is ready to receive new data.

8.2.8 BUSY: Busy

The busy signal indicates the printer is busy and not ready to receive new data.

8.2.9 PE: Paper End

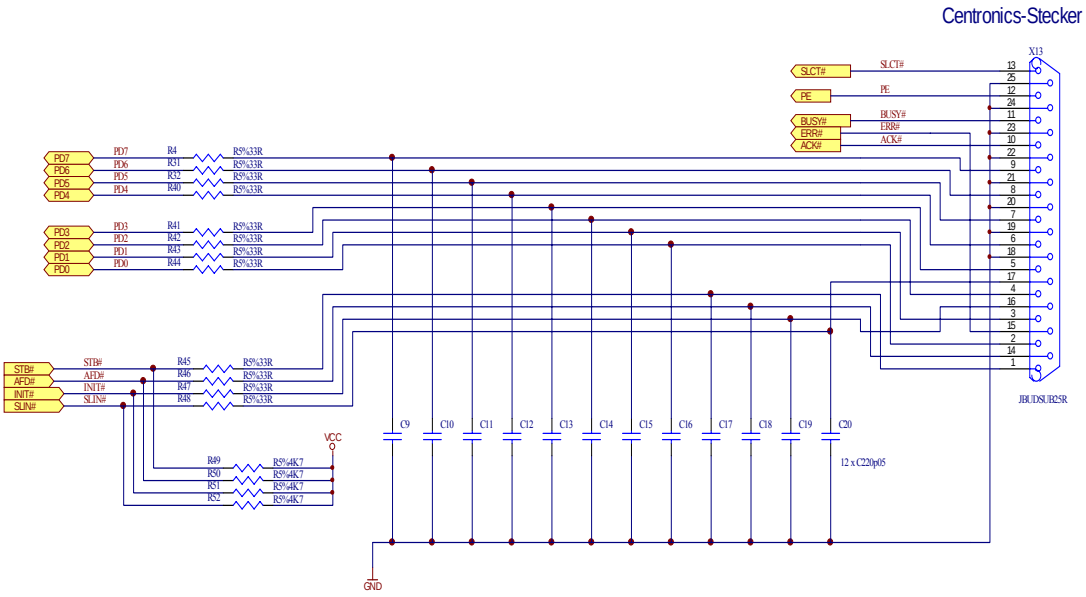
The PE signal indicates that the printer is out of paper.

8.2.10 SLCT: Printer Select Status

This active high output from the printer indicates that it has power on.

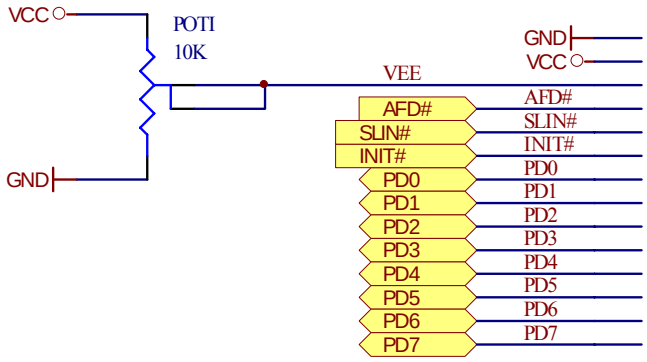
8.3 Design Example

8.3.1 Centronix Selector



8.3.2 Dot-Matrix Display

You can directly connect a standard dot-matrix display to the signals of printer port LPT1. For detailed pin descriptions, refer to the specifications from the manufacturer of the dot-matrix display.



Installing the Dot-Matrix Display

- ➤ Turn on or reboot the system.
- ➤ Press <DEL> if asked to enter setup.
- ➤ Change the settings for the LPT Port to Extended Mode.
- ➤ Save the settings and then start DOS.
- ➤ Start the program ALCDINIT, which is available at the Kontron Web site. When using a display with two rows and 16 columns, the correct command line for the program is:

  ```
  ALCDINIT COPY 16 2 00 40 00 40
  ```

- ➤ Reboot. Display is now ready for use. The LCD driving voltage (contrast) can be changed by a Potentiometer.

Note: *You cannot use a dot-matrix display and a printer simultaneously. If you want to use a printer, enter the BIOS setup menu and change the settings for the LPT Port to normal.*

9 Keyboard Interface

The DIMM-PC/520-I/IE/IU supports standard PC/AT style keyboards (AT and PS/2).

9.1 Configuration

BIOS configures the keyboard controller. The resources used by the keyboard controller are compatible with the PC/AT.

9.2 Signals

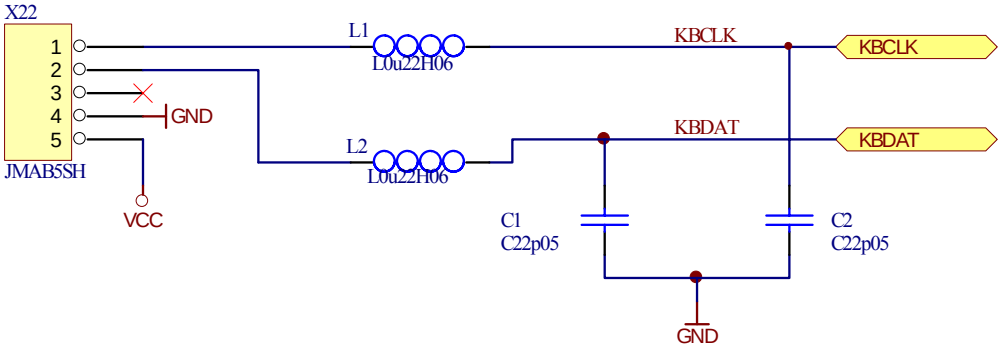
9.2.1 KBDAT: Keyboard Data

An open-collector output drives the bi-directional, keyboard-data signal.

9.2.2 KBCLK: Keyboard Clock

An open-collector output drives this keyboard-clock signal.

9.3 Design Example



10 Floppy Disk Interface

The floppy disk interface can support one drive. The drive may be 3.5" (720K, 1.44M, or 2.88M), or 5.25" (360K or 1.2M).

10.1 Configuration

The floppy disk controller (FDC) uses I/O, IRQ, and DMA resources. Configure the FDC in BIOS setup, choosing Disabled or Enabled. The resources used by the FDC are compatible with the PC/AT.

10.2 Signals

10.2.1 FDHDSEL# Head Select

The active low output determines the active disk-drive head.

10.2.2 FDRDATA: Read Data

The active low, data-read signal from the disk is connected here.

10.2.3 FDWRPRT: Write Protect

The active low input senses from the disk drive that a disk is write-protected.

10.2.4 FDTRK0#: Track 0 Indicator

The active low input senses from the disk drive that the head is positioned over the outermost track.

10.2.5 FDWGATE#: Write Gate

The active low output enables the write circuitry of the disk drive.

10.2.6 FDWDATA#: Write Data

The active low output is a write, pre-compensated serial data that will be written on a selected disk drive.

10.2.7 FDSTEP#: Head Step Signal

The active-low output produces a pulse at a software-programmable rate to move the head during a seek operation.

10.2.8 FDDIR#: Head Step Direction

The active low output determines the direction of the head movement.

10.2.9 FDMTR0#: Motor Enable Signal

The active low output selects the motor of the disk drive.

10.2.10 FDDSKCHG#: Floppy Disk Change Signal

The disk-interface input indicates when the disk-drive door has been opened.

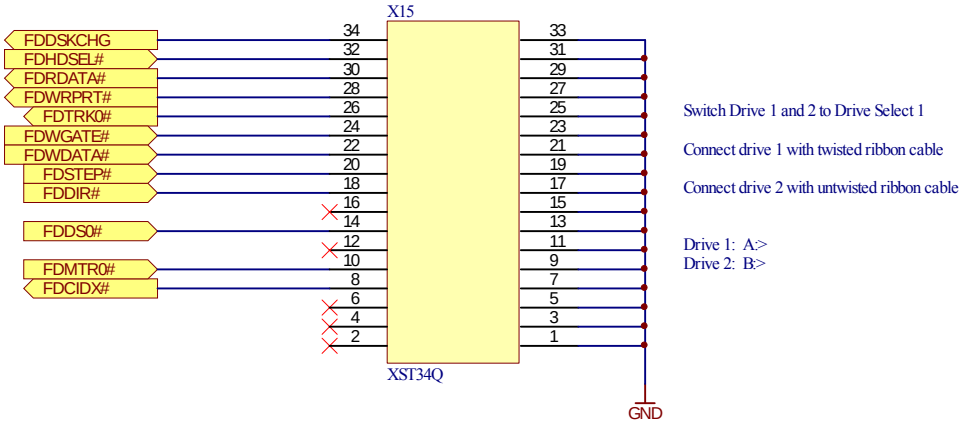
10.2.11 FDDS0#: Floppy Drive Select Signal

The active low output selects the disk drive.

10.2.12 FDCIDX#: Index Indicator

The active low input senses from the disk drive that the head is positioned over the beginning of a track, as marked by the index hole.

10.3 Design Example



11 IDE Hard-Disk Interface

11.1 Configuration

Configure the external hard disk as the slave. Always configure the onboard IDE-compatible Flash hard disk as master.

11.2 Signals

11.2.1 IDECS0#: IDE Chip Select 0

The hard disk chip select signal corresponds to the eight control-block addresses.

11.2.2 IDECS1#: IDE Chip Select 1

The hard disk chip select signal corresponds to the alternate status register.

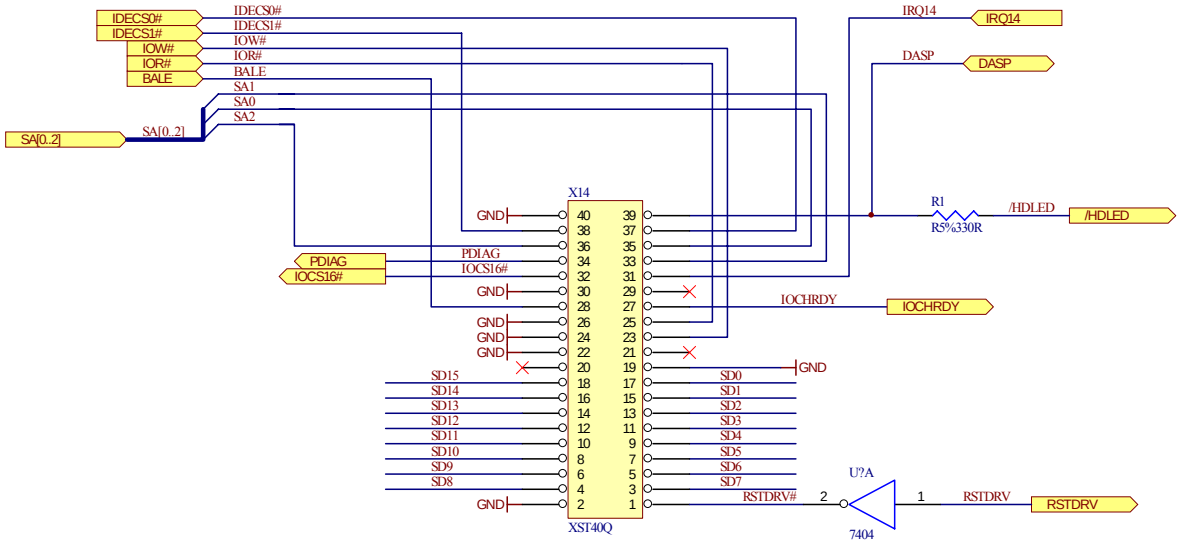
11.2.3 DASP

This time-multiplexed, open-collector, output signal indicates when a drive is active, or the presence of a slave drive.

11.2.4 PDIAG

This signal is used as output by the drive if it is jumped in the slave mode or as input to the drive if it is jumped in the master mode. The signal indicates to a master that the slave has passed its internal diagnostic command.

11.3 Design Example



12 USB Interface (Only available on DIMM-PC/520-IU)

One OHCI-type USB host controller is on the module. The USB controller complies with Version 1.1 of the USB standard. The implementation of this subsystem complies with the *DIMM-PC™ Specification*.

12.1 Configuration

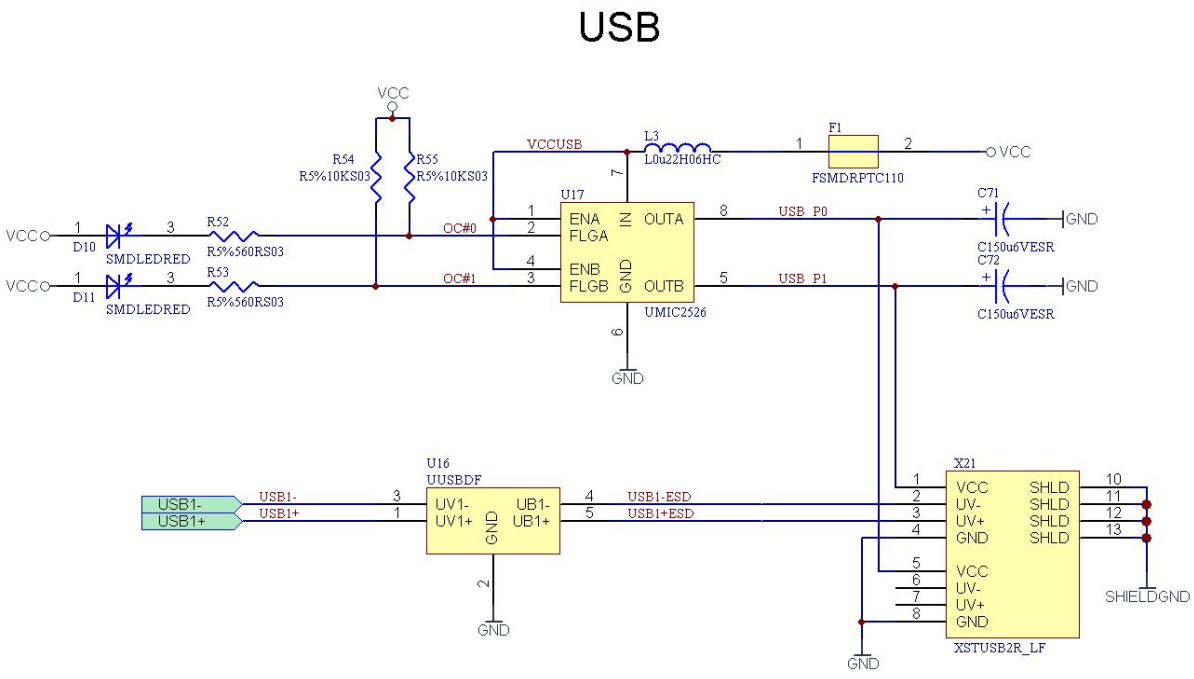
The USB controller is a PCI bus device. BIOS allocates required system resources during configuration of the PCI bus. The USB controller does not support USB legacy devices.

12.2 Signals

12.2.1 USB1+ / USB1-

Differential USB signal pair according to USB Specification 1.1.

12.3 Design Example



12.4 USB Boot

Booting from USB devices is not supported.

13 Ethernet Interface (Only available on DIMM-PC/520-IE)

The 82551ER is a fully integrated, cost-effective 10BASE-T LAN solution. It is designed for low-power use and high-performance processes. It is a 3.3V device with 5V tolerance and supports 3.3V and 5V signaling.

13.1 Configuration

The Ethernet controller is a PCI device. The BIOS setup automatically configures it.

13.2 Signals

13.2.1 TXD+ / TXD-

Differential transmit signal pair.

13.2.2 RXD+ / RXD-

Differential receive signal pair.

13.2.3 LKLED

Link status led

13.2.4 LNLED

Indicates activity on the line.

13.3 Design Example

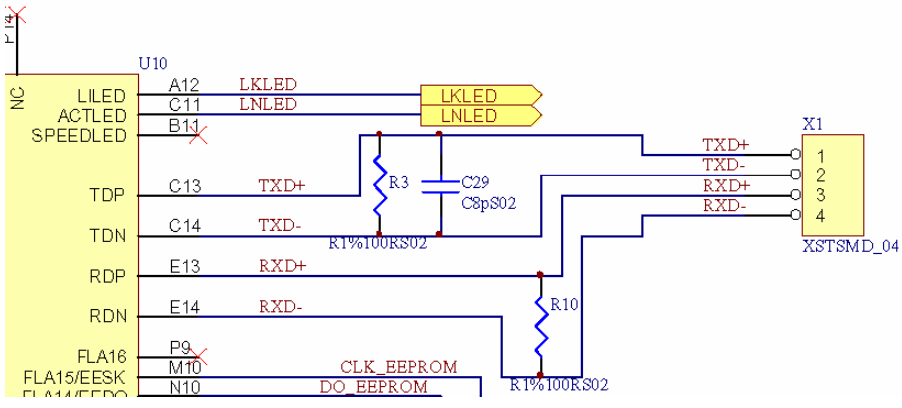


Figure 1 Ethernet connector on the CPU module.

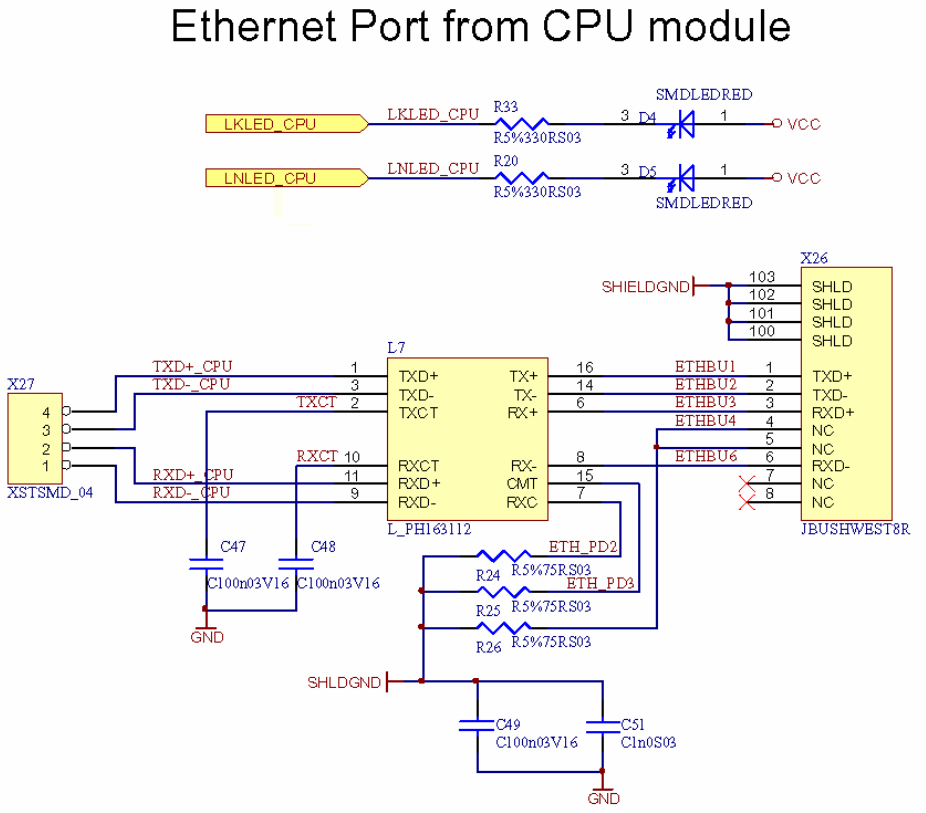
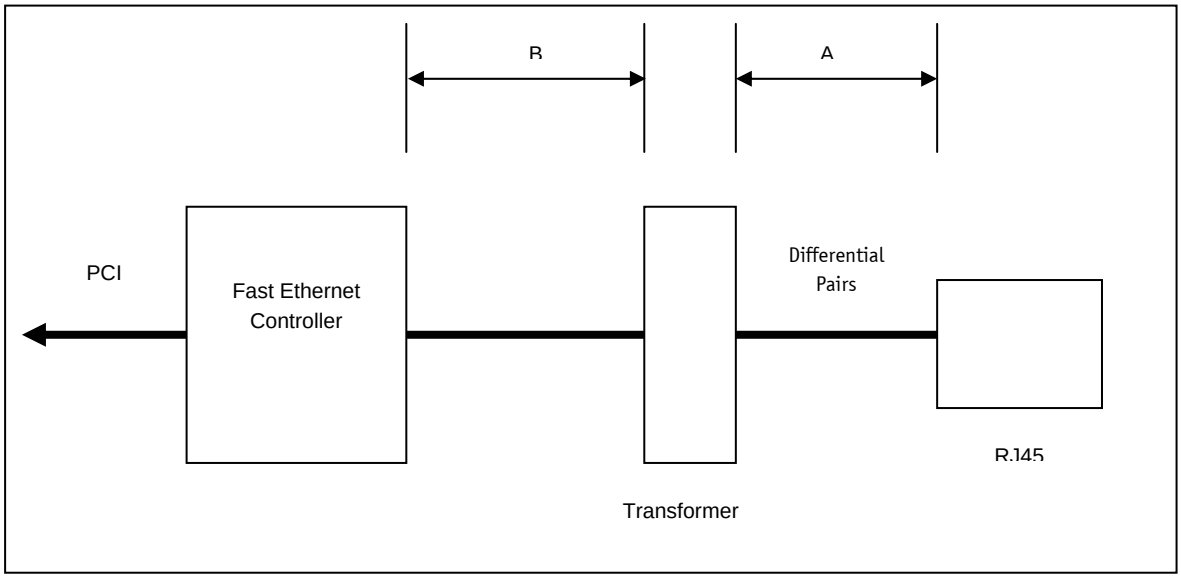


Figure 2 Ethernet connector (X27) on backplane to RJ45 connector on backplane.

13.4 Ethernet Implementation Notes



There are two critical dimensions that must be considered during the layout phase of an Ethernet controller. These dimensions are identified in the figure above as A and B.

Distance A: Transformer to RJ45 (Priority 1) The distance labeled "A" should be given the highest priority in the backplane layout. The distance between the transformer module and the RJ45 connector should be kept to less than 1 inch of separation. The following trace characteristics are important and should be observed:

1) Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance also can be affected by the spacing between the traces.

2) Trace Symmetry: Differential pairs (such as RXD and TXD) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Note: *Asymmetrical and unequal length traces in the differential pairs contribute to common mode noises. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the Ethernet controller must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping distance A as short as possible should be a priority.*

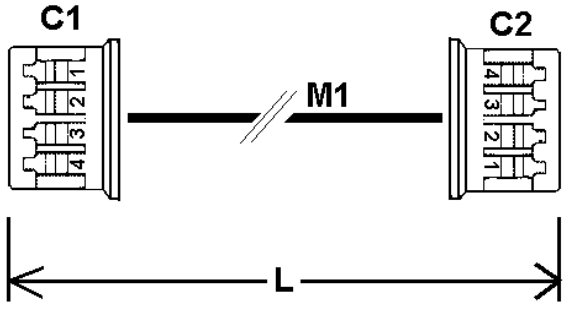
Distance B: PHY to Transformer (Priority 2) Distance B from Figure 20 should also be designed to extend as short as possible between devices. The high-speed nature of the signals propagating through these traces requires that the distances between these components be closely observed.

In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices.

Many board layouts have the –ground plane removed underneath the transformer and RJ45 jack to minimize capacitive coupling of noise between the plane and the external Ethernet cable. Link and activity LEDs can be implemented by using the DIMM module's LKLED and LNLED pins. These pins sink current and are intended for attachment to an LED cathode.

13.4.1 CPU Ethernet Connector Cable Information

Mechanical specification



Part list for KAB-JAEILZ-X-?? (?? Equals the length of the cable)

Part number	Manufacturer	Ordering Code	Description
C1, C2	JAE	IL-Z-4S-S125C3	JAE Wire-to-Board (4pos.) Receptacle Housing 1.25mm (.49“) Pitch
	JAE	IL-Z-C3-A-15000	Wire-to-Board Crimp Terminal
M 1	AMP	1-726822-0	Extruded Stranded Lead Ribbon Cable (??cm, 4pos.)

C1: CPU Module Ethernet Connector Pinout

PIN	Description
1	TXD+
2	TXD-
3	RXD+
4	RXD-

Connection Table

C1	C2
1	4
2	3
3	2
4	1

Note: *The Ethernet interface works according to the common criteria of the embedded technology market segment.*

13.4.2 Ethernet Limitation

According to the Physical Layer Specifications of IEEE802.3 an Ethernet controller should be able to drive a segment length of 100 m. Therefore most Ethernet controllers are designed to meet this requirement, if all Design & Layout Recommendations are met. However this is the point where problems arise for all modular standards for the following reasons:

- Due to the dimensions of the DIMM-PC standard the Ground Plane of the DIMM module often cannot be made as large as recommended
- Due to the direct proximity to other controllers with high frequent pulses the Ground Plane cannot be held as proper as recommended
- Due to the modular DIMM-PC concept the distance controller-magnetics will be longer than having controller-magnetics-jack on one board
- Due to the modular DIMM-PC concept a transmission line discontinuity occurs at the connectors modul-to-baseboard, attenuating the signal and reducing signal quality

Note:	*In consequence it may be possible that a DIMM-PC application will not be able to reach the mentioned 100 m limit. During the Product Release Process Kontron tests Ethernet transmission with 50 m Cable length. So this length can at least be reached with all Kontron DIMM-PC modules, proper baseboard design provided. More detailed information concerning Ethernet Transmission length with particular boards on request.*

14 Miscellaneous Interfaces

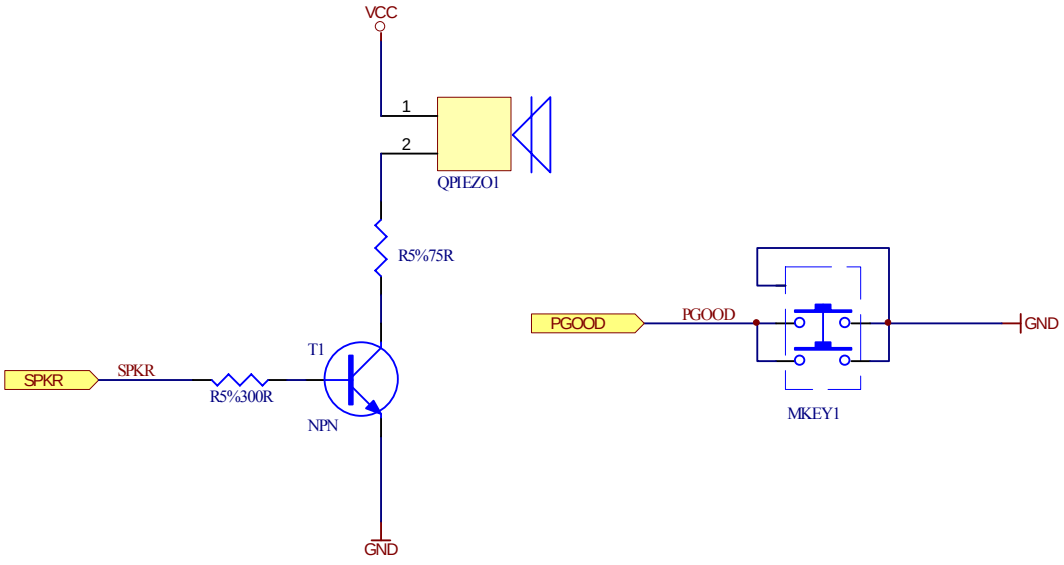
14.1 Speaker

You can connect an 8-Ohm loudspeaker between SPKR (Pin 134) and VCC (Pin 140).

14.1.1 SPKR: Speaker

Open the collector output on modules that drive a loudspeaker. An 8-Ohm loudspeaker connects between SPKR and VCC (+5V). Connect just one loudspeaker to this pin. The CPU typically drives this pin. However, other modules can use this signal to drive a system loudspeaker.

14.1.2 Design Example



14.2 Battery

The battery voltage has to be higher than 2.5 V and lower than 3.3V. A 3V battery is recommended.

You do not need a battery to maintain CMOS setup data.

14.2.1 BATT: System Battery Connection

This pin connects a system battery to all modules. The battery voltage has to be higher than 2.5V and lower than 3.3V. A 3V battery is recommended.

14.3 I2C-Bus

14.3.1 I2CLK: I2C-BUS CLK

The I2C-Bus Clock signal controls external I2C-bus slave devices.

14.3.2 I2DAT: I2C-BUS Data

The I2C-Bus Data signal controls external I2C-bus slave devices.

14.4 Power Good Reset

14.4.1 PGOOD: Power Good

A high-active input for the DIMM CPU indicates that power from the power supply is ready. You also can use this as a low active-reset input signal.

14.5 Serial Interrupt Request

14.5.1 SMISW SMI Interrupt Switch

This input generates the CPU's SMI interrupt.

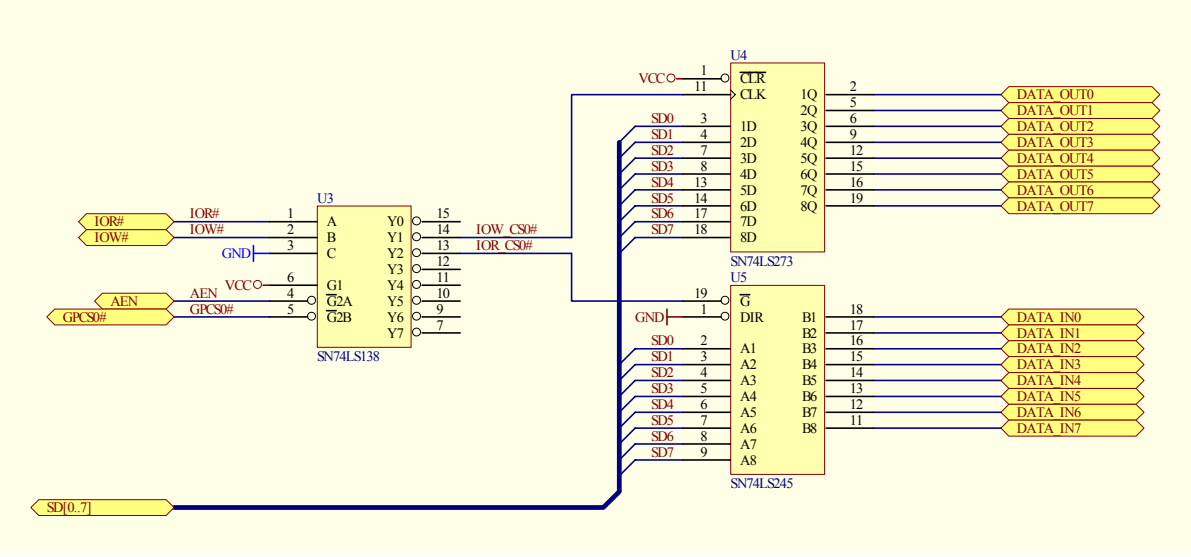
14.6 General Purpose Chip Select

The DIMM-PC/520-I/IE/IU offers a programmable chip select output, which is available over the DIMM-PC bus.

14.6.1 GPCS0#: General Purpose Chip Select

The GPCS0# selects external peripherals. From the BIOS setup, you can change or disable the I/O-port address of the chip select.

14.6.2 Design Example



15 Watchdog Timer

The DIMM-PC/520-I/IE/IU includes a Watchdog Timer (WDT) to ensure system integrity. When the WDT triggers, it can generate a RESET or a NMI.

15.1 Configuration

From the BIOS setup, you can configure the WDT mode and timeout.

15.2 Watchdog Extension

If you choose to use a 32 bit OS then you have to use JIDA32 API driver. The complete JIDA32 API driver and manual can be found on the Kontron web site. Under DOS you can easily control the Watchdog Extension with the aid of a special Interrupt 15h function.

The respective functions have the following calling conventions when using Interrupt 15h:

Watchdog init	Int 15h	00h
Input:	AH	= E0h
	AL	= 00h
	BX	= timeout in 0.2 sec increments
	CX	= None
	DX	= 0 = RESET, 1 = NMI
Output:	None	
Description:	Following values in BX are available : BX=0, Watchdog OFF This function is a public Kontron INT15h extension used to init the watchdog on Kontron boards.	

Note: *The timeout/delay granularity cannot be set in 0.2sec increments. It is adjusted to the following granularity: 0.5 sec, 1 sec, 2 sec, 4 sec and so on in double increments up to a maximum of 32 sec. Differing values are internally rounded up.*

Watchdog trigger	Int 15h	01h
Input:	AH	= E0h
	AL	= 01h
Output:	None	
Description:	This function is a public Kontron INT15h extension used to trigger the watchdog on Kontron boards.	

15.3 Detailed Description of Watchdog Function

15.3.1 Programming

The function *Init watchdog* must be called only once. The two parameters *timeout time* and *trigger event* must be set. The watchdog must be reset during the *timeout time* with the *trigger watchdog function*. Otherwise, a RESET or NMI will occur depending on *trigger event*.

The system BIOS makes it very easy to use the watchdog via software interrupt 15h. Two ways are possible to access the watchdog: The simplest way is to use AH=0E0h to init or trigger the watchdog.

```
Simple with AH = E0h
Init Watchdog (Int 15h, AH=E0h)
```

Called with AX E000h

BX **timeout time**

BX = 0 ⇨ watchdog off. BX_{max} = 0006h

CX **delay time**

CX = 0 ⇨ no delay supported!.

DX **trigger event**

DX = 0 ⇨ RESET, DX = 1 ⇨ NMI

Returns no

Example

```
mov   ax,0E000h     ; Watchdog set
mov   bx,5d         ; 1s Timeout
mov   cx,0          ; no Delay
mov   dx,0          ; after Timeout generate RESET
int   15h
```

16 Limitations

16.1 I/O Address Mapping

Only I/O addresses below 400h are mapped to the external ISA bus. The SC520 reserves all higher I/O addresses for the PCI

16.2 System Clock Deviation

In PC/AT compatible systems, the system boot code usually programs the Programmable Interval Timer Channel 0 Count (PIT0CNT) register (port 0040h) to a value of FFFFh. If the timer is based on the PC/AT standard clock of 1.19318 MHz, it results in a periodic IRQ0 generation (every 54.93 ms) to keep accurate time of day.

However, because the internal timer clock source of the SC520 is only 1.1892 MHz, setting the standard counter value results in a slower IRQ0 generation rate and subsequently an inaccurate time of day.

The DIMM-PC/520-I/IE/IU BIOS takes care of the deviating clock rate of the SC520 by setting the PIT0CNT to a value of FF25h. However, this only guarantees an accurate system clock for operating systems like DOS, which do not change the value set by the BIOS. If an operating system (such as Windows 98) re-initializes the PIT0CNT with the standard PC value of FFFFh, this will result in remarkable system clock deviation.

Setting the PIT0CNT to the DIMM-PC/520-I/IE/IU value of FF25h again after the operating system has started solves this problem.

16.3 Windows 2000 Support

Windows 2000 (an unmodified standard version) does not run on systems with ISA IDE controllers. During installation or start of a pre-installed system, Windows fails and displays the error message INACCESSIBLE_BOOT_DEVICE. As the DIMM-PC/520-I/IE/IU uses an ISA IDE interface, a standard Windows 2000 version cannot be installed or run on the DIMM-PC/520-I/IE/IU.

16.4 Watchdog NMI Handling

Although set to NMI mode, the SC520 watchdog will only generate a NMI for the first watchdog timeout. The next time the watchdog timer expires a reset will be generated.

To avoid this, the watchdog NMI interrupt service routine must clear bit 12 of the SC520 Watchdog Timer Control register by writing a 1 to this bit. The key sequence 3333h followed by CCCCh must be sent to the register (which is memory mapped to address E400:0CB0) before it can be write accessed. The following code sequence illustrates the described procedure:

```
.
.
unsigned int wdstore;
```

```
volatile unsigned int far *WDTMCTRL;
WDTMCTRL = ((void far *) 0xE4000CB0;
.
.
void interrupt NmiIsr (void)
{
      wdstore = *WDTMCTRL;
      *WDTMCTRL = 0x3333;
      *WDTMCTRL = 0xCCCC;
      wdstore = wdstore | 0x1000;
      *WDTMCTRL = wdstore
      .
      .
}
```

16.5 ISA SCSI Support

Because of limitations concerning 16Bit DMA transfers in conjunction with the asynchronous ISA bus timing, most ISA SCSI cards cannot be used with the DIMM-PC/520-I/IE/IU.

16.6 Video Support

ISA Graphic Adapters that depend on additional ports above 0400h for some special initialization cannot be used with the DIMM-PC/520-I/IE/IU.

17 Appendix A: System Resources

17.1 Interrupt Request Lines

IRQ #	Used for	Available
0	System Timer	No
1	Keyboard	No
2	Slave PIC	No
3	COM2	No (1)
4	COM1	No(1)
5		Yes
6	FDC	No(1)
7	LPT1	No(1)
8	Clock/Calendar	No
9	USB/Ethernet	No(2)
10	COM3	No(3)
11	COM4	No(3)
12		Yes
13	Numeric coprocessor	No
14	Hard Disk IDE0	No(1)
15		Yes

Notes: *([1]) If the "Used for" device is disabled in setup, the corresponding interrupt is available for other devices.*
([2]) When using a DIMM-PC/520-IU or DIMM-PC/520-IE the BIOS, by default, assigns IRQ 9 for the onboard Ethernet or USB controllers. You can change this assignment in the BIOS setup.
([3]) Unavailable if baseboard is equipped with an I/O controller SMC FDC37C669

17.2 Direct Memory Access Channels

DMA #	Used For	Available	Comment
0		Yes	
1		No	Note (2)
2	FDC	No	Note (1)
3		No	Note (3)
4	Cascade	No	
5		Yes	
6		No	Note (2)
7		No	Note (3)

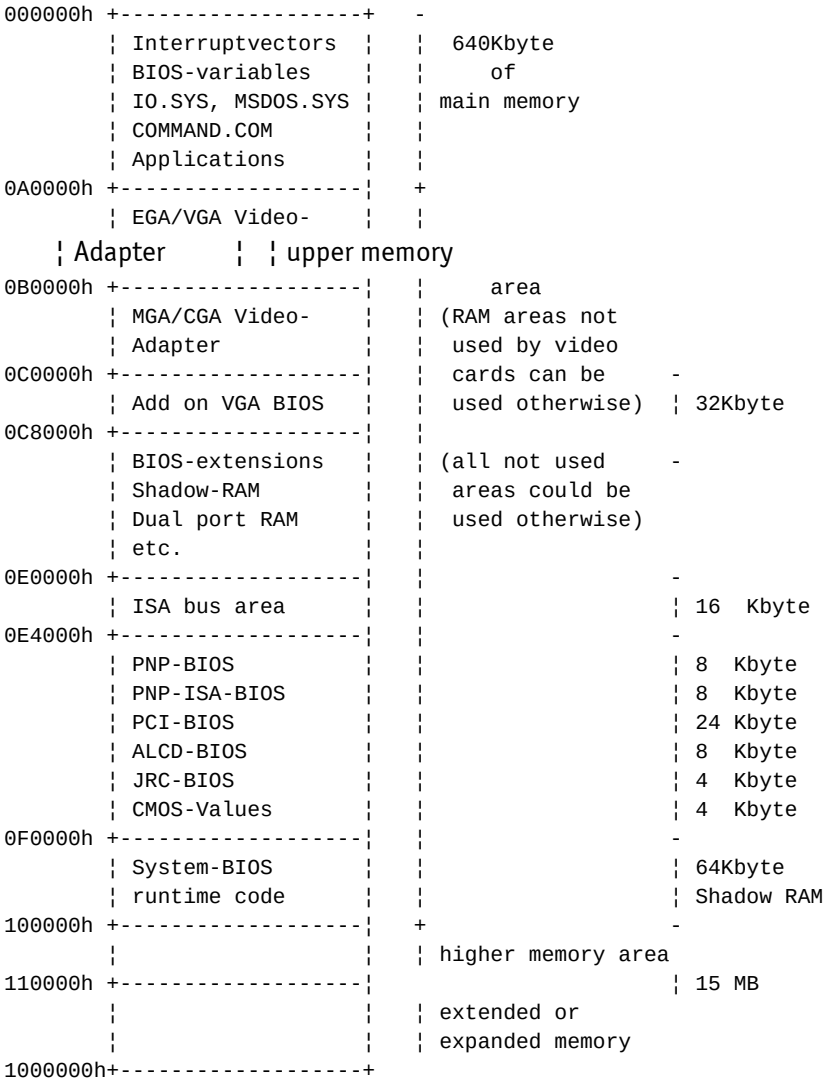
Notes: *(1) If the "Used for" device is disabled in setup, the corresponding channel is available for other devices.*
(2) Not available on the DIMM bus.
(3) Not available on DIMM-PC/520-I/IE/IU.

17.3 BIOS, ALCD, and JRC Memory Maps

The BIOS includes two extensions to support an alphanumeric dot matrix module (ALCD) on the parallel port and JRC. If the ALCD support is enabled or the JRC client finds a host, the code of the applicable BIOS extension will be copied to shadow RAM. The location where the BIOS extension is placed is determined by the system BIOS. You cannot influence this, exercise caution when Extended Memory Manager is used. To avoid memory conflicts, exclude the area E4000h-EFFFFh, and do not include the area C0000h-CFFFFh.

Using DOS, you can address 1MB directly. The memory area above 1MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS or EMM386.EXE. Other operating systems (OS/2, Windows NT) make it possible to address the full memory area directly.

17.3.1 Standard Memory Map



Note: The position of the ALCD and Remote Control BIOS extensions depends on the length of the VGA BIOS and the presence of BIOS extensions on the add-on cards. If no Remote Control host is found, you will be removed

from shadow RAM. The ALCD code only copies to shadow RAM if it is enabled in EEPROM.
On DIMM-PC/520-IE, there is a LAN boot ROM option available in the BIOS. This is a 38k ROM and if used this feature will be placed below address 0E4000h.

17.3.2 Expanded Memory Map

You can convert Extended Memory (up to 64Mb into Expanded Memory (EMS). The selected Expanded Memory is divided into 16KB pages, four of which can be mapped into the EMS frame. The EMS frame is located within the first 1MB address space and has a length of 64KB. The start address of the EMS page can be selected between C8000h and E0000h in steps of 16KB. Most Expanded Memory Managers choose their frame address locations independently, if it is not explicitly set.

```
000000h +-------------------+   -
        ¦ Interruptvectors  ¦   ¦  640Kbyte
        ¦ BIOS-variables    ¦   ¦     of
        ¦ IO.SYS, MSDOS.SYS ¦   ¦ main memory
          ¦ COMMAND.COM         ¦    ¦
        ¦ HIMEM, EMM386     ¦   ¦
        ¦ Applications      ¦   ¦
0A0000h +-------------------¦   +
        ¦ EGA/VGA Video-    ¦   ¦
        ¦ Adapter           ¦   ¦ upper memory
0B0000h +-------------------¦   ¦     area
        ¦ MGA/CGA Video-    ¦   ¦ (RAM areas not
        ¦ Adapter           ¦   ¦  used by video
0C0000h +-------------------¦   ¦  cards can be     -
        ¦ Add On VGA BIOS   ¦   ¦  used otherwise)  ¦ 64Kbyte
0C8000h +-------------------¦   ¦                   ¦ Shadow RAM
        ¦ BIOS-extensions   ¦   ¦ (all not used     -
        ¦ Shadow-RAM        ¦   ¦  areas could be
        ¦ Dual port RAM     ¦   ¦  used otherwise)
        ¦ EMS-Pages         ¦   ¦
        ¦ etc.              ¦   ¦
0E0000h +-------------------¦   ¦                   -
        ¦ ISA bus area      ¦   ¦                   ¦ 16  Kbyte
0E4000h +-------------------¦   ¦                   -
        ¦ PNP-BIOS          ¦   ¦                   ¦ 8  Kbyte
        ¦ PNP-ISA-BIOS      ¦   ¦                   ¦ 8  Kbyte
        ¦ PCI-BIOS          ¦   ¦                   ¦ 24 Kbyte
        ¦ ALCD-BIOS         ¦   ¦                   ¦ 8  Kbyte
        ¦ JRC-BIOS          ¦   ¦                   ¦ 4  Kbyte
        ¦ CMOS-Values       ¦   ¦                   ¦ 4  Kbyte
0F0000h +-------------------¦   ¦                   -
        ¦ System-BIOS       ¦   ¦                   ¦ 64Kbyte
        ¦ runtime code      ¦   ¦                   ¦ Shadow RAM
100000h +-------------------¦   +                   -
        ¦                   ¦   ¦ higher memory area
110000h +-------------------¦   +
        ¦                   ¦   ¦ extended or
        ¦                   ¦   ¦ expanded memory
```

To work with Expanded Memory under MS-DOS, add the following drivers to CONFIG.SYS:

- HIMEM.SYS
- EMM386.EXE

The DIMM-PC/520-I/IE/IU uses two BIOS extensions (for Remote Control and ALCD support), which are dynamically copied into shadow memory (if Remote Control host found resp., ALCD enabled). Other boards have no extension BIOS but use drivers that communicate with their corresponding devices via memory mapped I/O. Such boards share the upper memory area with the Expanded Memory Manager. This is often the reason for several problems in the system. Make sure you exclude all areas in the upper memory that are used by extension BIOSes and memory mapped I/O. The instructions in the CONFIG.SYS concerning the Expanded Memory Manager should look similar to the following: (question marks indicate the location of extension BIOS).

DEVICE=EMM386.EXE X=E400-EFFF

17.4 DIMM-PC Bus Connector Pinout

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	IOCHCK#	2	GND	3	RSTDRV
4	IDECS0#	5	SD7	6	VCC
7	SD6	8	IDECS1#	9	IRQ9
10	DASP	11	SD5	12	PDIAG
13	SD4	14	DTR2#	15	DRQ2
16	RI2#	17	SD3	18	TXD2
19	SD2	20	CTS2#	21	MEMCS16#
22	RXD2	23	SD1	24	RTS2#
25	0WS# (***)	26	DCD2#	27	IOCS16#
28	GND	29	SD0	30	DSR2#
31	SBHE#	32	FDHDSEL#	33	IOCHRDY
34	FDRDATA#	35	IRQ10	36	FDWRPRT#
37	AEN	38	FDTRK0#	39	SMEMW#
40	FDWGATE#	41	IRQ11	42	FDWDATA#
43	SA19	44	FDSTEP#	45	SMEMR#
46	FDDIR#	47	IRQ12	48	FDMTR0#
49	SA18	50	FDDSKCHG	51	IOW#
52	FDDS0#	53	IRQ15	54	FDIDX#
55	SA17	56	USB1- (*)	57	IOR#
58	GND	59	IRQ14	60	SA16
61	DACK0#	62	GND	63	SA15
64	USB1+ (*)	65	DRQ0	66	VCC
67	SA14	68	LNLED (**)	69	DACK5#
70	LKLED (**)	71	SA13	72	I2CDAT
73	DRQ5	74	I2CCLK	75	SA12
76	GPCS0#	77	REF#	78	DCD1#
79	SD8	80	DSR1#	81	SA11
82	RXD1	83	SYSCLK	84	RTS1#
85	SD9	86	TXD1	87	SA10
88	CTS1#	89	IRQ7	90	GND
91	SD10	92	DTR1#	93	SA9
94	RI1#	95	IRQ6	96	STB#
97	SD11	98	AFD#	99	SA8
100	PD0	101	IRQ5	102	ERR#
103	SD12	104	PD1	105	SA7
106	INIT#	107	IRQ4	108	PD2
109	DACK7# (***)	110	SLIN#	111	DRQ7 (***)
112	PD3	113	IRQ3	114	PD4
115	SA6	116	PD5	117	SD13
118	PD6	119	DACK2#	120	PD7
121	SA5	122	ACK#	123	SD14
124	BUSY	125	TC	126	PE
127	SA4	128	SLCT#	129	SD15
130	KBDAT	131	BALE	132	KBCLK
133	SA3	134	SPKR	135	MASTER# (***)
136	PGOOD	137	SA2	138	SMISW
139	SA1	140	VCC	141	OSC
142	BATT	143	SA0	144	GND

Note: *(*) Only available on the DIMM-PC/520-IU.*
(**) Only available on the DIMM-PC/520-IE
(***) Unavailable on all versions of DIMM-PC/520

17.5 I/O Map

The I/O port addresses of the processor module DIMM-PC/520-I/IE/IU are functionally identical to a standard PC/AT.

I/O Addresses	DIMM-PC/520-I/IE/IU	Function
0000 - 0–1F	x	DMA Controller 1
0020 - 0–3F	x	Interrupt Controller 1
0040 - 0–43	x	Timer
0050 - 0–5F	x	Onboard Control Registers
0060 - 0–64	x	Keyboard Controller
0061	x	Port B Register
0070	x	NMI Enable Register
0070 - 0–71	x	Real-time Clock
0080 - 0–8F	x	DMA Page Register 74LS612
0092	x	Port A Register (Fast A20 Gate)
00A0 - 0–BF	x	Interrupt Controller 2
00C0 - 0–DF	x	DMA Controller 2
00F0 - 0–FF	x	Math Coprocessor
0100		I/O Channel
0110	x	General Purpose Chip Select
01F0 - 0–F7	x	Fixed Disk
0200 – 0207		Game I/O
020C-020D		Reserved
021F		Reserved
0220	x	General Purpose Chip Select
0278 - 0–7F		Parallel Port 2
02B0 - 0–DF		Alternate Enhanced Graphics Adapter
02E1		GPIB (Adapter 0)
02E2 - 0–E3		Data Acquisition (Adapter 0)
02F8 - 0–FF	x	Serial Port 2
0300 - 0–0F		Onboard Network (default configuration)
0310 - 0–1F		Prototype Card
0330	x	General Purpose Chip Select
0360 – 0363		PC Network (low address)
0364 – 0367		Reserved
0368 - 0–6B		PC Network (high address)
036C - 0–6F		Reserved
0378 - 0–7F	x	Parallel Port 1
0380 - 0–8F		SDLC, Bisynchronous 2
0390 – 0393		Cluster
03A0 - 0–AF		Bisynchronous 1
03B0 - 0–BF		Monochrome Display and Printer Adapter
03C0 - 0–CF		Enhanced Graphics Adapter
03D0 - 0–DF		Color/Graphic Monitor Adapter
03F0 - 0–F7	x	Diskette Controller
03F8 - 0–FF	x	Serial Port 1

18 Appendix B: BIOS Operation

The DIMM-PC/520-I/IE/IU is equipped with a JUMPtec (Kontron) Embedded BIOS, which is located in a Flash EEPROM onboard. This device has an 8-bit wide access. The shadow RAM feature (default) provides faster access. For a detailed description of the BIOS setup, refer to the section below. You can update the BIOS using a Flash utility.

18.1 Determining BIOS Version

To determine the BIOS version, immediately press the <**Pause**> key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

PhoenixBIOS 4.0 Release 6.0

Copyright 1985-2001 Phoenix Technology Ltd.

All Rights Reserved

Kontron(R) BIOS Version <D501R115>

(C)opyright 2003 Kontron(R) Embedded Modules GmbH

18.2 Setup Guide

The Phoenix BIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

The BIOS setup menus documented in this section represent those found in most modules. The BIOS setup for specific models can differ slightly.

Note: *Selecting incorrect values may cause system boot failure. Load setup-default values to recover by pressing <F9>.*

18.2.1 Start Phoenix BIOS Setup Utility

To start the Phoenix BIOS Setup Utility, press the <**F2**> key when the following string appears during boot up.

Press <F2> to enter Setup

The Main Menu then appears.

18.2.2 General Information

The **Setup Screen** is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top-level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and - k–ys to select a value for that field. The **Save Value** commands in the **Exit** menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing **<F1>** or **<ALT-F1>** on a menu brings up the General Help window that describes the legend keys and their alternates. Press **<Esc>** to exit the General Help window.

18.3 Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Set system time. Use <Enter> to move to MM or SS.
System Date	MM/DD/YYYY	Set system date. Use <Enter> to move to DD or YYYY.
Legacy Diskette A	360kB, 5¼ "1.2 MB, 5 ¼ "720 kB, 3 ½ " **1.44/1.25 MB**, 3 ½ "2.88 MB, 3 ½ " Not Installed Disabled	Select type of floppy-disk drive.
▶Primary Master	Autodetected drive	Displays result of PM autotyping.
▶Primary Slave	Autodetected drive	Displays result of PS autotyping.
▶Secondary Master	Autodetected drive	Displays result of SM autotyping.
▶Secondary Slave	Autodetected drive	Displays result of SS autotyping.
▶Memory Shadow	submenu	Opens Memory Shadow submenu.
System Memory	N/A	Displays amount of conventional memory detected during bootup.
Extended Memory	N/A	Displays amount of extended memory detected during bootup.

Note: *In the Option column, bold shows default settings.*

18.4 Master or Slave Submenus

Feature	Option	Description
Type	None User **Auto** CD-ROM	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies the hdd information. Auto = Autotyping, the drive itself supplies the information's-ROM = CD-ROM drive.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity (CHS)	N/A	Displays calculated size CHS drive.
Total Sectors	N/A	Total number of sectors in LBA mode.
Maximum Capacity (LBA)	N/A	Displays calculated size of the drive in LBA.
Multi-Sector Transfer	Disabled Standard 2 sectors 4 sectors 8 sectors **16 sectors**	Any selection except Disabled determines the number of sectors transferred per block. The standard is 1 sector per block.
LBA Mode Control	Disabled **Enabled**	Enabling Logical Block Addressing allows use of LBA instead of CHS.

Note: *In the Option column, bold shows default settings.*

18.4.1 Memory Shadow Submenu

Feature	Option	Description
Video Shadow	Disabled **Enabled**	Enables/disables shadowing of video ROM.
C800 – CFFF	**Disabled** Enabled	Accesses to the upper memory region go to the ISA bus if Disabled or to local memory if Enabled. This option is not displayed if VGA BIOS exceeds 32kB. In that case, this region is shadowed automatically.
D000 – D7FF	**Disabled** Enabled	See above.
D800 – DFFF	**Disabled** Enabled	See above.

Note: *In the Option column, bold shows default settings.*

18.5 Advanced Menu

Feature	Option	Description
▶Advanced Chipset Control	Submenu	Opens Advanced Chipset Control submenu.
▶PCI Configuration	Submenu	Opens PCI Configuration submenu.
Plug & Play OS	Yes **No**	If your system has a PNP OS (e.g. Win95) select 'Yes' to let the OS configure PNP devices not required for boot. 'No' makes the BIOS configure them.
Reset Configuration Data	**No** Yes	'Yes' erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select 'Yes' when required to restore manufacturer defaults.
▶Keyboard Features	Submenu	Opens Keyboard Features submenu.
▶I/O Device Configuration	Submenu	Opens I/O Device Configuration submenu.
Large Disk Access Mode	**DOS** Other	Select 'DOS' if you have DOS. Select 'Other' if you have another OS such as UNIX. A large disk has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.
Halt On Errors	**Yes** No	Determines if post errors cause system to halt.

Note: *In the Option column, bold shows default settings.*

18.5.1 Advanced Chipset Control Submenu

Feature	Option	Description
CPU Speed	100 MHz **133 MHz**	Select CPU frequency.
Cache Mode	**Write Back** Write Through	Select SC520 L1 cache mode.
CAS latency	**3T** 2T	Select CAS latency.
RAS to CAS delay	2T **3T**	Select RAS to CAS delay.

	4T	
RAS Precharge time	2T **3T** 4T 6T	Select RAS precharge time.
Refresh cycle time	7.8 us **15.6 us** 31.2 us 62.5 us	Select SDRAM refresh cycle time.
SDRAM buffer	Disabled **Enabled**	The integrated SDRAM read/write buffer increases overall system performance.
ISA bus cycle duration	400ns **800 ns** 1.2us2us	Set duration of a complete ISA bus cycle.
IOCHCHK configuration	**Signal ignored** Assert NMI	Enables IOCHCHK signal to assert an NMI

Note: In the Option column, bold shows default settings.

18.5.2 PCI Configuration Submenu

Feature	Option	Description
PCI concurrent mode	Disabled **Enabled**	In concurrent mode, direct PCI to PCI transfers do not require gaining ownership of the CPU-memory host bus. Thus PCI transfers are accelerated.
Park PCI on CPU*	Disabled **Enabled**	Enabled: The PCI bus is parked on the CPU after a PCI transaction. Disabled: The PCI bus is parked on the last PCI master.
CPU PCI master priority*	**1** 2 3	The CPU is granted the PCI bus after the selected number of external PCI master cycles.
Delay Transaction*	Disabled **Enabled**	Enabled maximizes PCI bus efficiency by freeing up the bus while initial SDRAM read is issued.
Host-PCI Write Buffer*	Disabled **Enabled**	Maximizes host write accesses to PCI.
PCI IRQ line 3	Disabled, **Auto Select**, 3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Select IRQ for PCI interrupt INTC (used for onboard USB or Ethernet controller).
▶PCI/PNP ISA UMB Region Exclusion	Submenu	Opens UMB Region Exclusion submenu.
▶PCI/PNP ISA IRQ Resource Exclusion	Submenu	Opens IRQ Exclusion submenu.

Note: *In the Option column, bold shows default settings.*
** Only visible if PCI concurrent mode is set to Enabled.*

18.5.3 PCI/PNP ISA UMB Region Exclusion Submenu

Feature	Option	Description
C800 –CBFF	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
CC00 – CFFF	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
D000 – D3FF	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
D400 – D7FF	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
D800 – DBFF	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
DC00 - D–FF	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.

18.5.4 PCI/PNP ISA IRQ Exclusion Submenu

Feature	Option	Description
IRQ 3	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ 4	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ 5	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ 7	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ 9	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ 10	**Available** Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
IRQ 11	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ 12	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ 15	**Available** Reserved	Reserves the specified IRQ for use by legacy ISA devices.

Note: *In the Option column, bold shows default settings.*

18.5.5 Keyboard Features Submenu

Feature	Option	Description
Numlock	**Auto** On Off	On or Off turns NumLock on or off at bootup. Auto turns NumLock on if it finds a numeric keypad.
Key Click	**Disabled** Enabled	Turns audible key click on.
Keyboard auto-repeat rate	**30/sec** 26.7/sec	Sets the number of times to repeat a keystroke per second if you hold the key down.

	21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	
Keyboard auto-repeat delay	¼ sec **½ sec** ¾ sec 1 sec	Sets delay time after the key is pressed before it begins to repeat the keystroke.

Note: *In the Option column, bold shows default settings.*

18.5.6 I/O Device Configuration Submenu

Feature	Option	Description
Local Bus IDE Adapter	Disabled **Enabled**	Enables onboard IDE device.
Floppy disk controller	Disabled **Enabled** Auto	Enables onboard FDC controller.
Base I/O address	**Primary** Secondary	Selects base address of onboard FDC controller. (Primary = 3F0h, Secondary = 370)
Serial Port A Serial Port B Serial Port C* Serial Port D*	Disabled **Enabled** Auto	'Disabled' turns off the port. 'Enabled' requires end user to enter the base I/O address and the IRQ. 'Auto' makes BIOS configure the port.
Mode (only port D)	**Normal** IrDA Ask-IR	Selects mode of Serial Port D (if enabled.)
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h	Select I/O base serial ports.
IRQ	IRQ3 (Port A and B) IRQ4 (Port A and B) IRQ10 (Port A, C and D) IRQ 11 (Port B, C and D)	Select IRQs of serial ports.
Parallel Port	Disabled Enabled **Auto**	'Disabled' turns off port. 'Enabled' requires end user to enter the base I/O address and IRQ. 'Auto' allows BIOS to configure the port.
Mode	Output only **Bi-directional** ECP EPP	Set mode of the parallel port.
Base I/O address	378h, 278h, 3BCh	Select I/O base of port.
IRQ	IRQ 5, IRQ 7	Select IRQ of parallel port.
DMA	DMA 1, 3	Select DMA channel of port if in ECP mode.
▶Watchdog Setting	Submenu	Opens Watchdog Settings submenu.
ISA memory gap	**Disabled** Enabled	Enabled allows to map a memory area to the ISA bus. Must be set to Disabled to set additional ISA I/O area 2.
ISA memory gap base (MB)	8 – 15	Define the base address of the ISA memory gap on MByte boundaries. The minimum value for the gap base is 8MByte,

		the maximum value is 15MByte. Gap base + gap size may not exceed the 16MByte ISA bus memory limit.
ISA memory gap size (MB)	1 – 8	Define the size of the ISA memory gap in MByte. Minimum gap size is 1MByte, maximum gap size is 8MByte. Gap base + gap size may not exceed the 16MByte ISA bus memory limit.
Additional ISA I/O area 1	**Disabled** Enabled	Per default the SC520 directs I/O accesses above 400h to PCI. This node allows to configure an additional ISA I/O area above 400h. Plug&Play ISA cards will not work if this node is set to Enabled.
Base address	400h – FFFFh **400h**	Define the base address of the additional ISA I/O area 1. Only values above 400h are accepted.
Range (bytes)	1 – 512 **512**	Define the size of the additional ISA I/O area 1, up to 512 bytes.
Additional ISA I/O area 2	**Disabled** Enabled	Per default the SC520 directs I/O accesses above 400h to PCI. This node allows to configure an additional ISA I/O area above 400h. Must be disabled to set the ISA memory gap.
Base address	400h – FFFFh **600h**	Define the base address of the additional ISA I/O area 2. Only values above 400h are accepted.
Range (bytes)	1 – 512 **512**	Define the size of the additional ISA I/O area 2, up to 512 bytes.
Additional ISA I/O area 3	**Disabled** Enabled	Per default the SC520 directs I/O accesses above 400h to PCI. This node allows to configure an additional ISA I/O area above 400h. Must be Disabled to use the I/O Chip Select feature.
Base address	400h – FFFFh **800h**	Define the base address of the additional ISA I/O area 3. Only values above 400h are accepted.
Range (bytes)	1 – 512 **512**	Define the size of the additional ISA I/O area 3, up to 512 bytes.
►I/O Chip Select	Submenu	Opens general purpose I/O chip select submenu.

Note: *In the Option column, bold shows default settings.*
** Only available if Super I/O SMC 669 is detected; otherwise, the menus are hidden.*

18.5.7 Watchdog Settings Submenu

Feature	Option	Description
Mode	**Disabled** ResetNMI	Select watchdog operation mode.
Delay	No Delay 0.5s, 1s, 2s, **4s**, 8s, 16s, 32s	The time until the watchdog counter starts counting. Useful to handle longer boot times.
Timeout	0.5s, 1s, 2s, **4s**, 8s, 16s, 32s	Max. trigger period.

Note: *In the Option column, bold shows default settings.*

18.5.8 I/O Chip Select Submenu

Feature	Option	Description
I/O Base	**Disabled** 110h 220h 330h	Select general-purpose I/O chip; select base address.
Range in Bytes	4, 8	Address range in bytes covered by I/O chip select.

18.6 Security Menu

Feature	Option	Description
Set User Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password restricts setup access.
Set Supervisor Password	Up to seven alphanumeric characters	Pressing <Enter> displays a dialog box for entering a user password. In related systems, this password allows full setup access.
Password on boot	**Disabled** Enabled	'Enabled' requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.
Diskette access	User **Supervisor**	Enabled requires supervisor password to access floppy disk.
Fixed disk boot sector	**Normal** Write protected	Write protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Virus check reminder System backup reminder	**Disabled** Daily Weekly Monthly	Displays a message during bootup asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with „Y". 'Daily' displays the message on the first boot of the day, 'Weekly' on the first boot after Sunday, and 'Monthly' on the first boot of the month.

Notes: *In the Option column, bold shows default settings.*
Enabling Supervisor Password requires a password for entering Setup.
Passwords are not case sensitive.
User and Supervisor passwords are related.
You can only create a user password if a supervisor password exists.

18.7 Boot Menu

Feature	Option	Description
Floppy check	**Disabled** Enabled	'Enabled' verifies floppy type on boot; 'disabled' speeds boot.
Summary screen	**Disabled** Enabled	If enabled, a summary screen is displayed just before booting the OS to let the end user see the system configuration.
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This decreases time needed to boot the system.
Dark Boot	**Disabled** Enabled	If enabled, system comes up with a blank screen instead of the diagnostic screen during bootup.
▶Boot Device Priority	Submenu	Opens boot device priority submenu.
Onboard LAN RPL ROM	**Disabled** Enabled	Enables Remote Program Load ROM of the **onboard** LAN controller (if available). Supports Intel PXE.

18.7.1 Boot Device Priority Submenu

This menu allows you to select the order of the devices from which the BIOS attempts to boot the OS. During POST, if BIOS is unsuccessful at booting from one device, it will try the next one on the list.

Each item on this menu can represent the first of a class of items. For example, if you have more than one hard-disk drive, Hard Drive represents the first of such drives as specified in the Hard Drive menu described below.

To change the order, select the device you want to change and press <-> to decrease or <+> to increase priority.

Feature	Option	Description
▶Removable Devices	Boot priority & submenu	Sets boot priority of Removable Devices as described in the respective submenu.
▶Hard Drives	Boot priority & submenu	Sets boot priority of Hard Disks as described in the respective submenu.
ATAPI CD-ROM Drive	Boot priority	Sets boot priority of ATAPI CD: ROM Drives.
▶Network Boot	Boot priority & submenu	Sets boot priority of Network Adapters as described in the respective submenu.

Removable Devices Menu

If you have more than one Removable Media drive, select Removable Devices and press <Enter> to display the Removable Media menu. Choose which drive is represented in boot-order menu. The standard 1.44MB floppy drive is referenced as „Legacy Floppy Drives."

Hard Drive Priority Menu

If you have more than one bootable hard drive, select Hard Drive and press <Enter> to display the Fixed Disk Menu and choose the boot priority.

Network Boot Priority Menu

If you have more than one bootable network adapter in the system, select Network Boot and press <Enter> to display the available network adapters and choose the boot priority.

Boot First Menu

Display the Boot First Menu by pressing <Esc> during POST. In response, the BIOS first displays the message „Entering Boot Menu...Ind then displays the Boot Menu at the end of POST.

Use the menu to select any of these options:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to the previous boot sequence.
- Enter Setup.
- Press <Esc> to continue with the existing boot sequence.

18.8 Exit Menu

The following sections describe the five options in **Exit Menu**. Pressing **<Esc>** does not exit this menu. You must select an item from the menu to exit.

Exit Saving Changes

Saves all selections and exits setup. Upon reboot, the BIOS configures the system according to the Setup selection stored in CMOS.

Exit Discarding Changes

Exits Setup without storing new selections in CMOS. Previous selections remain in effect.

Load Setup Defaults

Select to display default values for all Setup menus.

Discard Changes

Discards changes made during a Setup session and revert to values previously saved in CMOS.

Save Changes

Saves all selections without exiting Setup.

18.9 Updating or Restoring BIOS

If your board requires a newer BIOS version or the BIOS is damaged, you may need to update or restore the BIOS.

Phoenix PHLASH allows you to update or restore the BIOS with a newer version or restore a corrupt BIOS by using a floppy disk without having to install a new ROM chip.

1. Download Phoenix Phlash as a compressed file, CRISD501.ZIP, from the Kontron Web site. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the Flash ROM.
WINCRISIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRISIS.HLP	Serves as the help file of WINCRISES.EXE.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

2. To install Phoenix Phlash on a hard disk, unzip the content of CRISD501.ZIP into a local directory such as C:\PHLASH.

3. To create a Crisis Recovery Diskette, insert a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the Crisis Recovery Diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the Flash ROM.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the BIOS image to be programmed into Flash ROM.

4. If the BIOS image (BIOS.ROM) changes because of an update or bug fix, copy the new BIOS.ROM image onto the diskette.

5. Phlash can fail if the system uses memory managers. If this occurs, the utility displays the following message:

Cannot flash when memory managers are present.

If you see this message after you execute Phlash, disable the memory manager.

18.10 Preventing Problems When Updating or Restoring BIOS

Updating the BIOS represents a potential hazard. Power failures or fluctuations that can occur during updating the Flash ROM can damage the BIOS code, making the system unbootable.

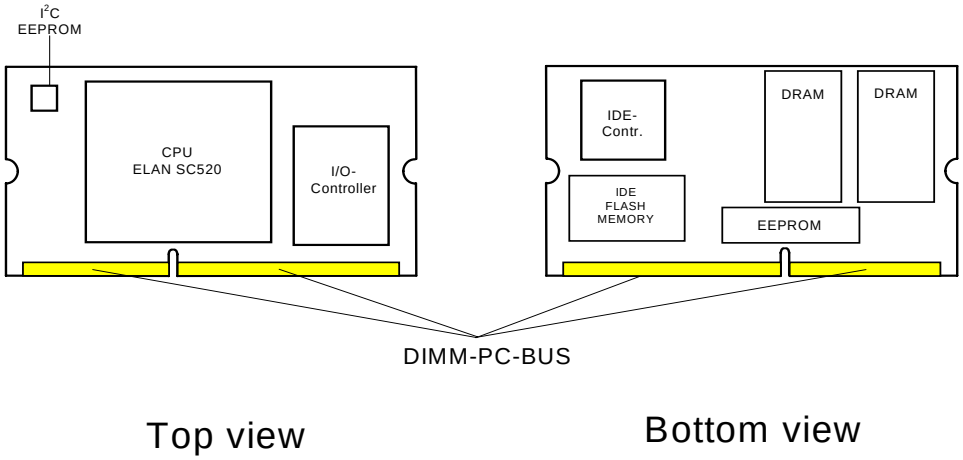
To prevent this potential hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

Additionally, you can insert an update key into the serial port (COM1 only) to force initiating the recovery routine for the boot block.

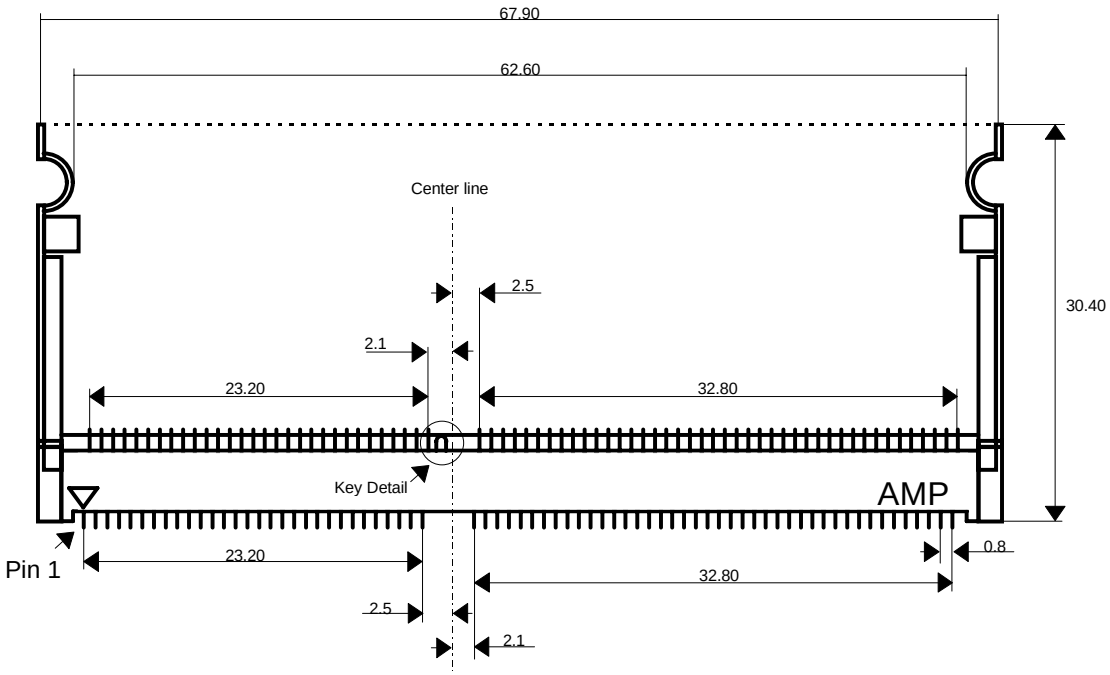
For further information on the update key and the crisis diskette, see a special application note PHLASH_EC_1XX.PDF, which is available from the Kontron Web site at http://emea.kontron.com/index.php?id=82&cat=34

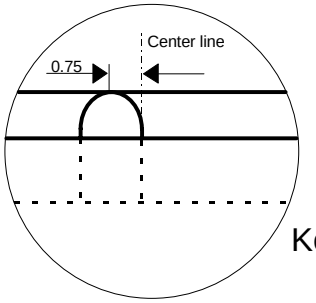
19 Appendix C: Connectors

19.1 DIMM-PC Bus

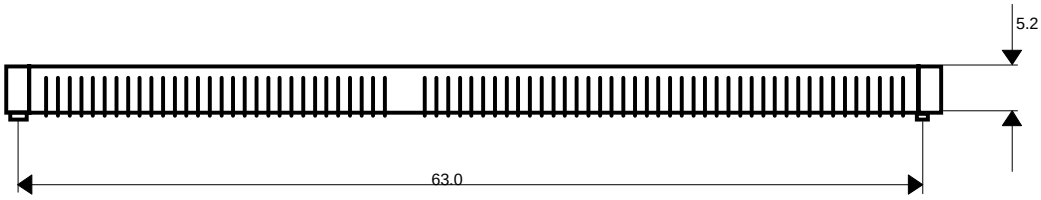


19.2 Mating Socket



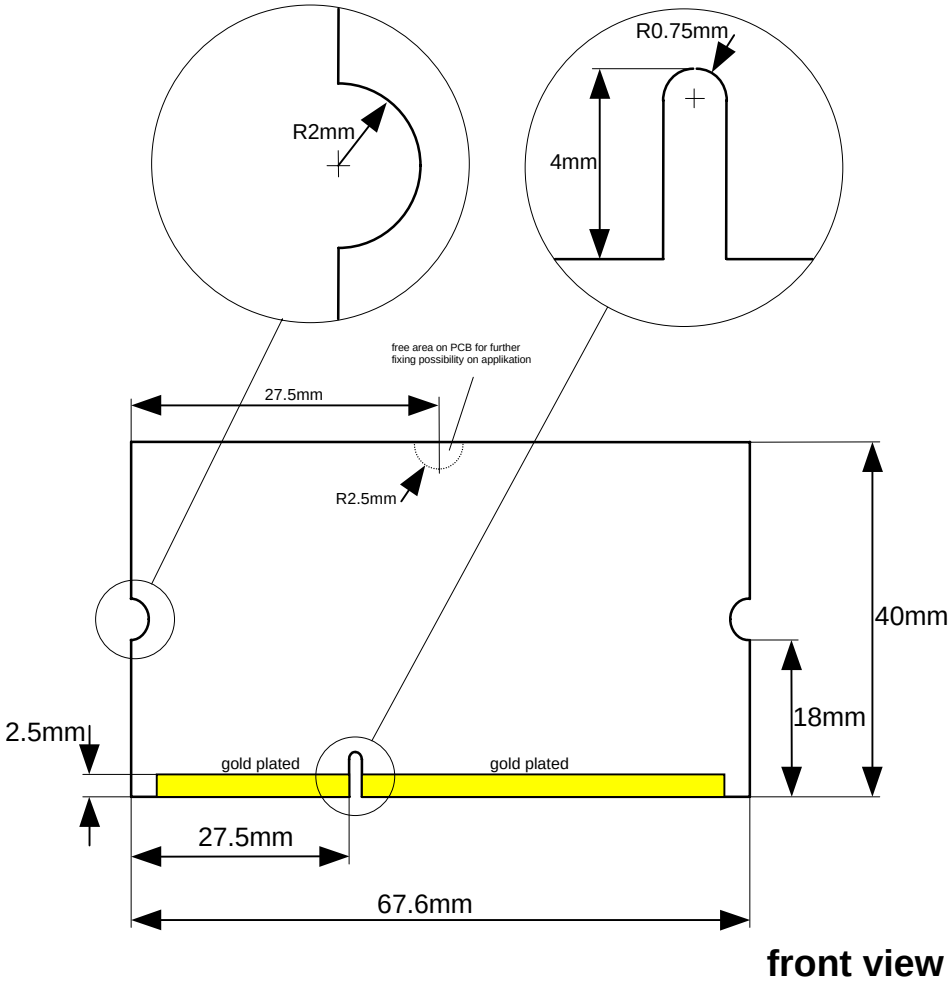


Key Detail (Type C)

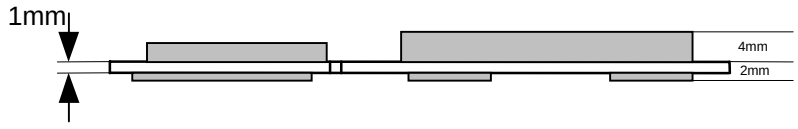


20 Appendix D: Mechanical Dimensions

20.1 Front and Side View



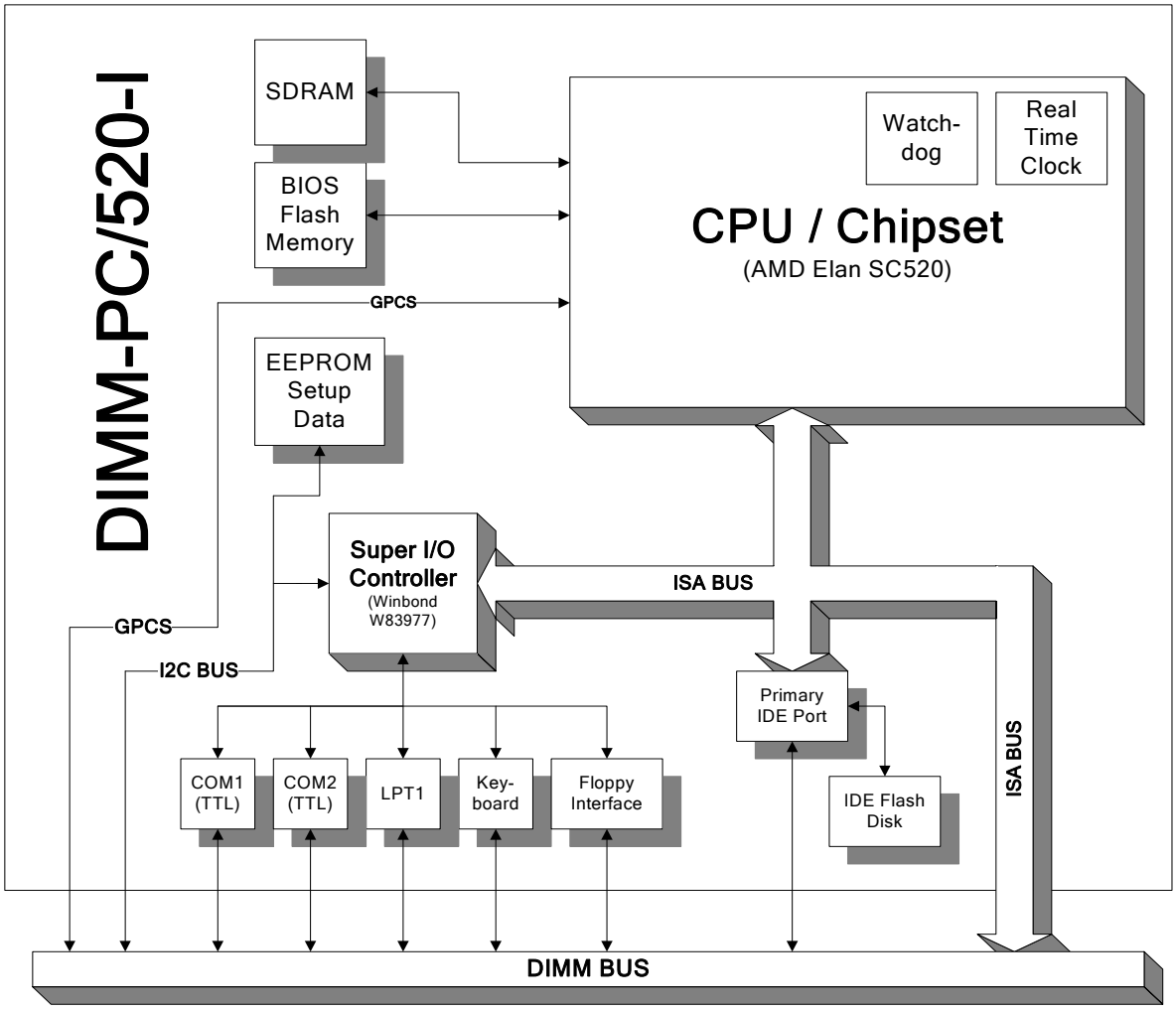
front view



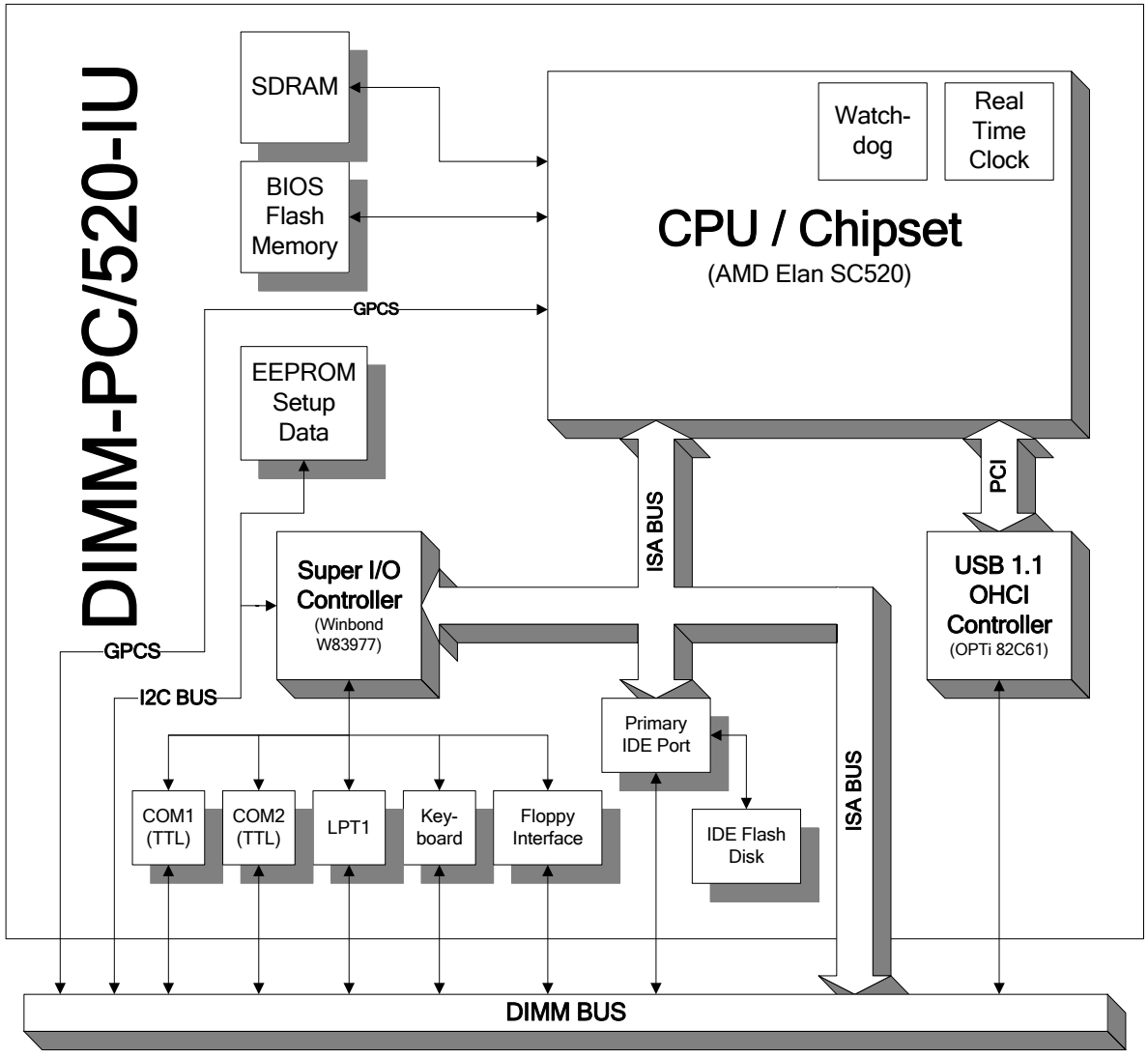
side view

21 Appendix E: block diagrams

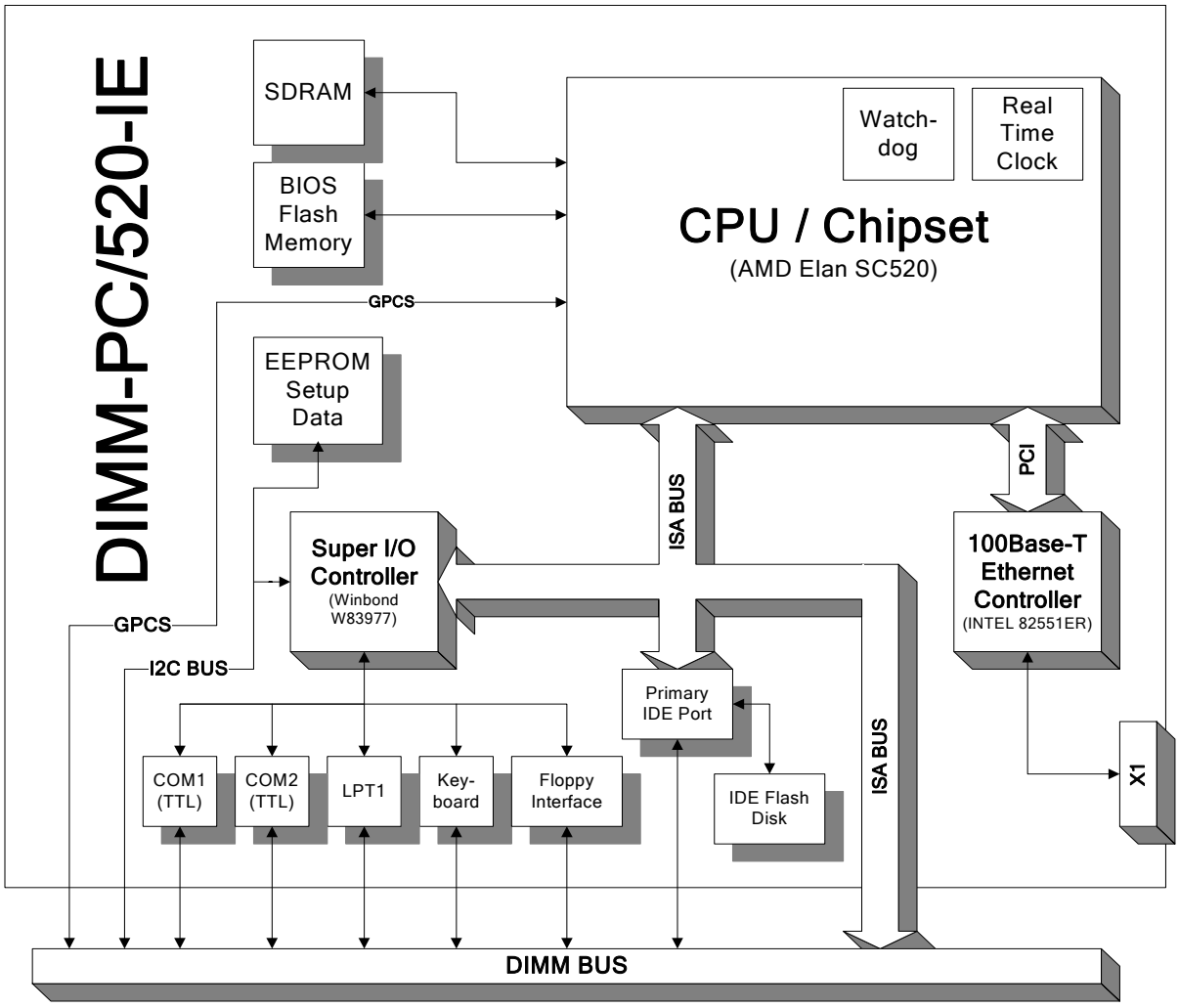
21.1 DIMM-PC/520-I



21.2 DIMM-PC/520-IU



21.3 DIMM-PC/520-IE



22 Appendix F: JIDA Standard

22.1 Calling Convention

Every board with an onboard BIOS extension supports the following function calls, which supply information about the board. JUMP*tec* Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=EAh
- aL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL≠0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

22.2 Obtaining JIDA Information

To obtain information about boards that follow the JIDA standard:

- Call Get BIOS ID with CL=1.
  The name of the first device installed will be returned.
  If you see the result **Board exists** (CL=0), increment CL, and call **Get BIOS ID** again.
- Repeat until you see **Board not present** (CL≠0).
  You now know the names of all boards within your system that follow the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: *Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.*

Refer to the JIDA manual in the jidai110.zip file, which is available from the Kontron Web site, for further information on implementing and using JIDA calls with C sample code.

23 Appendix G: JUMPTEC Remote Control

The JUMPtec Remote Control (JRC), an extension of the PC BIOS, provides a way to intercept and reroute BIOS functionality over a serial port at an early stage during booting.

There are two software components involved:

- The BIOS extension. The PC that contains this component is referred to as a client. This component is part of the JUMPtec (Kontron) Extension BIOS.
- Application. The second component runs on a different machine, which is referred to as a host, and is connected with a serial cable to a client. The second component is an application that can run at the command prompt or from batch files. The component is available as a 32-bit Windows console for Windows 9x or NT and as an MS-DOS application.

You can configure the interception in one of two ways:

- Server Mode provides a way of intercepting screen output from and keyboard input to the client on the host machine. In Server Mode, you can map the host's floppy drive to the client's drive-specifier A:. The host also can emulate a single disk drive as a file on the host machine's hard disk. Create this file using the command IMGCREATE. The file is accessible from the client machine as Drive A:.
- Image Mode allows you to halt the boot process of the client. This allows the host machine to read or write the contents of the CMOS RAM, EEPROM CMOS mirror, and NVRAMs of other Kontron boards as well as the contents of flash, hard, or floppy disks of the client.

For further information, see Application Note JRCUsage_Exxx.pdf, which is available from the Kontron Web site under Tech Support.

24 Appendix H: PC Architecture Information

The following sources of information can help you better understand DIMM-PC architecture.

24.1 DIMM-PC Specification

- DIMM-PC Specification, www.kontron.com

24.2 PC/104-Bus

- PC/104 Specification Version 2.3 June 1996
- PC/104 Consortium; www.pc104.org
- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)

24.3 ISA-Bus, Standard PS/2 - Connectors

- ISA System Architecture, Addison-Wesley Publishing Company
- Edward Solari, AT BUS Design IEEE P996 Compatible, Annabooks San Diego CA. ISBN 0-929392-08-6 www.annabooks.com
- PC Handbook, Sixth Edition, John P. Choisser and John O. Foster, Annabooks San Diego CA. ISBN 0-929392-36-1 www.annabooks.com
- AT IBM Technical Reference Vol 1&2, 1985
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)

24.4 RS232C, RS485

- EIA-232-E Interface between data terminal equipment and date circuit-terminating equipment employing serial binary data interchange (ANSI/IEA-232-D)
- EIA-422-A Electrical characteristics of balanced voltage digital interface circuits
- EIA-423-A Electrical characteristics of unbalanced voltage digital interface circuits
- EIA-485 Standard for electrical characteristics of generators and receivers for use in balanced digital multipoint systems
- EIA-449 General purpose 37-position and 9-position interface for data terminal equipment and data circuit-terminating equipment.
- EIA-530 High speed 25-position interface for data terminal equipment and data circuit-terminating equipment
- EIA/TIA-562 Electrical characteristics for an unbalanced digital interface

- National Semiconductor's Interface Data Book includes any applications notes. These notes are also available online at http://www.national.com/. A search engine is provided to search the text of the available application notes. Entering „232“, „422“ or „485“ as search criteria to get a current list of related application notes.

24.5 PC Hardware

- PC Hardware, Messmer Hans-Peter, Addison-Wesley-Longman GmbH, 1998, ISBN 3-8273-1302-3 (German)

25 APPENDIX I: DOCUMENT-REVISION HISTORY

Revision	Date	Edited by	Alteration to Preceding Revision
D501M110.DOC	27.06.01	BAJ	Preliminary manual created.
D501M111.DOC	26.08.01	GWE	BIOS and JIDA description updated; limitations section added.
D501M112.DOC	05.09.02	GUL	Updated SDRAM Flash hard-disk size; DMA limitation.
D501M113.DOC	05.09.02	HUM	Logo changed.
D501M114.DOC	22.08.03	GDA and JL	Updated technical information throughout manual.
D501M115.DOC	02.09.03	GDA	Updated section 14.2 with proper Battery information.
D501M116.DOC	18.12.03	GDA	Changed block diagram for IE version and corrected watchdog timeout information.
D501M117.DOC	12.02.04	GDA	Added web site link to Technical Support section. Changed reference from Phlash_EC_Exxx.doc to Phlash_EC_E1xx.pdf
D501M118.DOC	09.03.04	GDA	Removed references to 100 Base T Ethernet, DIMM-PC/520/IE only supports 10 Base T Ethernet.
D501M119.DOC	28.10.04	GDA	Changed value of section 3.3.4 from Maximum to Nominal value.
D501M120.DOC	28.10.04	GDA	Design example in section 14.6.2 was incorrect. Replaced it with correct design example.
D501M121.DOC	10.02.05	GDA	In section 18.5 Plug and Play OS was listed twice, removed second entry.
D501M122.doc	09.06.05	GUL	Removed I2C-Bus from CPU/Chipset and connected to Super-I/O Controller
D501M123.DOC	23.08.05 09.09.05 30.09.05	GUL HRU GUL	Removed: Battery-RTC information Added note for Ethernet limitation Released for WEB
D501M124.DOC	30.11.05 25.04.06 26.04.06	SMA GUL GUL	Added IOCHCHK setup node description Updated Support Adresses Updated to new Kontron style Corrected USB design example Released for WEB
D501M125.DOC	16.01.06	STO	Add Ethernet Limitation
D501M126.doc	23.04.07	GUL	Updated new Kontron Style